

# CS-200: Verilog Coding Style Guide

**Learning Goal:** Verilog Style.

**Requirements:** Verible.

## 1 Introduction

This document will teach you some guidelines for a readable and well-constituted Verilog.

We will use [Verible](#) as the linting tool for the labs. The tool does not cover all of the rules in this document; however, it comes in handy in detecting many problems that might exist in your Verilog code. We will run Verible on each submission and will **deduct half of the lab grade** if the code does not pass the linting with zero errors. We provide a `flags.txt` file alongside this document that shall be used as a configuration input to the Verible linter. The content of the `flags.txt` file can be found below with the command needed to run the linter on a Verilog file.

```
-always-comb
+port-name-suffix
signal-name-style="style_regex:[a-z_0-9]+'"
-explicit-parameter-storage-type
+parameter-name-style="localparam_style:ALL_CAPS;parameter_style:ALL_CAPS"
```

```
verible-verilog-lint {file} --rules_config flags.txt
```

## 2 General Guidelines

- **always@ (\*)** is used to describe a block with combinational logic. The `*` symbol is used in the sensitivity list to trigger the block whenever any of the inputs are changed; therefore, the outputs reflect the inputs change.
- **always@ (posedge clk)** is used to describe a block with sequential logic i.e., has flip-flops. The two keywords **posedge** and **negedge** determine whether the active clock edge of the flip-flops is the rising or the falling clock edge respectively.
- Use blocking (`=`) assignments in **combinational** always blocks.
- Use nonblocking (`<=`) assignments in **edge-sensitive sequential** always blocks. Blocking assignments (`=`) are not allowed.
- Avoid latches in your sequential designs and use only D flip-flops. Latches might sneak into your combinational blocks; to avoid this, it is a good practice to start your combinational always block

# Verilog Style Guide

**Padhraic Smyth**



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