

Figure P3.10:

Since gate voltage is high, the midpoint V, is expected to be low. Therefore, the load is in saturation and the driver is in linear region. From KCL

Using the following two equations to iterate find the solution,

The intermediate values are listed in the table:

$-\mathbf{V}_{T,k}(\mathbf{V}_s)$	V <sub>x</sub>
0.480	0.1523
0.518	0.1337
0.513	0.1359
0.514	0.1357
0.514	0.1357

3.11 The following parameters are given for an nMOS process:

$$t_{\rm m}=16~{\rm A}$$
  
substrate doping  $N_{\rm s}=4\cdot10^{10}~{\rm cm}^{\circ}$   
polysilicon gate doping  $N_{\rm p}=2\cdot10^{20}~{\rm cm}^{\circ}$   
exide-interface fixed-charge density  $N_{\rm m}=2\cdot10^{10}~{\rm cm}^{\circ}$ 

- (a) Calculate V<sub>s</sub> for an unimplanted transistor.
- (b) What type and what concentration of impurities must be implanted to achieve  $V_p = +0.6$  V and  $V_p = -0.6$  V?

# **Solution Manual Digital Integrated Circuit Hodges**

**Yi-Tong Ma** 

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