

**UNIT I: INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS**

9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

**UNIT II: RETIMING, ALGORITHMIC STRENGTH REDUCTION**

9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

**UNIT III: FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS**

9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

**UNIT IV: SCALING, ROUND-OFF NOISE, BIT-LEVEL ARITHMETIC ARCHITECTURES**

9

Scaling and round-off noise – scaling operation, round-off noise, state variable description of digital filters, scaling and round-off noise computation, round-off noise in pipelined IIR filters, Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

**UNIT V: NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING**

9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining, Asynchronous pipelining, bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

**REFERENCES:**

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, Second Edition, 2004.

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VLSI Signal Processing, VI IEEE Acoustics, Speech, and Signal Processing Society,1993      VLSI and Modern Signal Processing ,      VLSI Signal Processing Architectures Institution of Electrical Engineers. Electronics Division. Professional Groups E10 (Circuit Theory and Design), E4 (Image Processing and Vision) and E5 (Signal Processing),1990      VLSI Analog Signal Processing Circuits Hongjiang Song,2014-02-14 This book is based on a collection of the past exams for the VLSI Analog Signal Processing Circuits class EEE598 the author offered in the School of Engineering at Arizona State University The topics cover various aspects of the design analysis and application of VLSI analog signal processing circuits This book is intended to be used together with the VLSI Analog Signal Processing Circuits textbook by the same author It can also be used alone for the experienced readers      **Digital Signal Processing for VLSI** Institution of Electrical Engineers. Electronics Division. Professional Group E10 (Circuit Theory and Design),1988      *VLSI Signal Processing Systems* Earl E. Swartzlander,1986      VLSI Signal Processing, II Sun Yuan Kung,Robert E. Owen,J. Greg Nash,1986      Vlsi Design Methodologies For Digital Signal Processing Architectures Bayoumi,2005-01-01      VLSI systems design for digital signal processing B. A. Bowen,William Roy Brown,1985

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