

Bruce Jacob

The Memory System

You Can't Avoid It, You Can't Ignore It, You Can't Fake It



The Memory System Bruce Jacob

Abhishek Bhattacharjee, Daniel Lustig

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Memory Systems Bruce Jacob, David Wang, Spencer Ng, 2010-07-28 Is your memory hierarchy stopping your microprocessor from performing at the high level it should be Memory Systems Cache DRAM Disk shows you how to resolve this problem The book tells you everything you need to know about the logical design and operation physical design and operation performance characteristics and resulting design trade offs and the energy consumption of modern memory hierarchies You learn how to to tackle the challenging optimization problems that result from the side effects that can appear at any point in the entire hierarchy As a result you will be able to design and emulate the entire memory hierarchy Understand all levels of the system hierarchy Xcache DRAM and disk Evaluate the system level effects of all design choices Model performance and energy consumption for each component in the memory hierarchy The Memory System Bruce Jacob, 2009-07-08 Today computer system optimization at both the hardware and software levels must consider the details of the memory system in its analysis failing to do so yields systems that are increasingly inefficient as those systems become more complex This lecture seeks to introduce the reader to the most important details of the memory system it targets both computer scientists and computer engineers in industry and in academia Roughly speaking computer scientists are the users of the memory system and computer engineers are the designers of the memory system Both can benefit tremendously from a basic understanding of how the memory system really works the computer scientist will be better equipped to create algorithms that perform well and the computer engineer will be better equipped to design systems that approach the optimal given the resource limitations Currently there is consensus among architecture researchers that the memory system is the bottleneck and this consensus has held for over a decade Somewhat inexplicably most of the research in the field is still directed toward improving the CPU to better tolerate a slow memory system as opposed to addressing the weaknesses of the memory system directly This lecture should get the bulk of the computer science and computer engineering population up the steep part of the learning curve Not every CS CE researcher developer needs to do work in the memory system but just as a carpenter can do his job more efficiently if he knows a little of architecture and an architect can do his job more efficiently if he knows a little of carpentry giving the CS CE worlds better intuition about the memory system should help them build better systems both software and hardware Table of Contents Primers It Must Be Modeled Accurately and It Will Change Soon The Memory System Bruce Jacob, 2009-06-19 Today computer system optimization at both the hardware and software levels must consider the details of the memory system in its analysis failing to do so yields systems that are increasingly inefficient as those systems become more complex This lecture seeks to introduce the reader to the most important details of the memory system it targets both computer scientists and computer engineers in industry and in academia Roughly speaking computer scientists are the users of the memory system and computer engineers are the designers of the memory system Both can benefit tremendously from a basic understanding of how the memory system really

works the computer scientist will be better equipped to create algorithms that perform well and the computer engineer will be better equipped to design systems that approach the optimal given the resource limitations Currently there is consensus among architecture researchers that the memory system is the bottleneck and this consensus has held for over a decade Somewhat inexplicably most of the research in the field is still directed toward improving the CPU to better tolerate a slow memory system as opposed to addressing the weaknesses of the memory system directly This lecture should get the bulk of the computer science and computer engineering population up the steep part of the learning curve Not every CS CE researcher developer needs to do work in the memory system but just as a carpenter can do his job more efficiently if he knows a little of architecture and an architect can do his job more efficiently if he knows a little of carpentry giving the CS CE worlds better intuition about the memory system should help them build better systems both software and hardware Table of Contents Primers It Must Be Modeled Accurately and It Will Change Soon The Memory System Bruce Jacob, Sadagopan Srinivasan, David T. Wang, 2009 Introduce the reader to the most important details of the memory system This book targets both computer scientists and computer engineers in industry and in academia Roughly speaking computer scientists are the users of the memory system and computer engineers are the designers of the memory system Both can benefit tremendously from a basic understanding of how the memory system really works The Computer Engineering Handbook Vojin G. Oklobdzija, 2001-12-26 There is arguably no field in greater need of a comprehensive handbook than computer engineering The unparalleled rate of technological advancement the explosion of computer applications and the now in progress migration to a wireless world have made it difficult for engineers to keep up with all the developments in specialties outside their own References published only a few years ago are now sorely out of date The Computer Engineering Handbook changes all of that Under the leadership of Vojin Oklobdzija and a stellar editorial board some of the industry's foremost experts have joined forces to create what promises to be the definitive resource for computer design and engineering Instead of focusing on basic introductory material it forms a comprehensive state of the art review of the field s most recent achievements outstanding issues and future directions The world of computer engineering is vast and evolving so rapidly that what is cutting edge today may be obsolete in a few months While exploring the new developments trends and future directions of the field The Computer Engineering Handbook captures what is fundamental and of lasting value

Cache and Memory Hierarchy Design Steven A. Przybylski,1990 A widely read and authoritative book for hardware and software designers This innovative book exposes the characteristics of performance optimal single and multi level cache hierarchies by approaching the cache design process through the novel perspective of minimizing execution time Digital Systems and Applications Vojin G. Oklobdzija,2017-12-19 New design architectures in computer systems have surpassed industry expectations Limits which were once thought of as fundamental have now been broken Digital Systems and Applications details these innovations in systems design as well as cutting edge applications that are emerging to take

advantage of the fields increasingly sophisticated capabilities. This book features new chapters on parallelizing iterative heuristics stream and wireless processors and lightweight embedded systems This fundamental text Provides a clear focus on computer systems architecture and applications Takes a top level view of system organization before moving on to architectural and organizational concepts such as superscalar and vector processor VLIW architecture as well as new trends in multithreading and multiprocessing includes an entire section dedicated to embedded systems and their applications Discusses topics such as digital signal processing applications circuit implementation aspects parallel I O algorithms and operating systems Concludes with a look at new and future directions in computing Features articles that describe diverse aspects of computer usage and potentials for use Details implementation and performance enhancing techniques such as branch prediction register renaming and virtual memory Includes a section on new directions in computing and their penetration into many new fields and aspects of our daily lives Portable Electronics: World Class Designs John Donovan, 2009-03-12 All the design and development inspiration and direction an electronics engineer needs in one blockbuster book John Donovan Editor in Chief Portable Design has selected the very best electronic design material from the Newnes portfolio and has compiled it into this volume. The result is a book covering the gamut of electronic design from design fundamentals to low power approaches with a strong pragmatic emphasis In addition to specific design techniques and practices this book also discusses various approaches to solving electronic design problems and how to successfully apply theory to actual design tasks The material has been selected for its timelessness as well as for its relevance to contemporary electronic design issues Contents Chapter 1 System Resource Partitioning and Code OptimizationChapter 2 Low Power Design Techniques Design Methodology and ToolsChapter 3 System Level Approach to Energy ConservationChapter 4 Radio Communication BasicsChapter 5 Applications and TechnologiesChapter 6 RF Design ToolsChapter 7 On Memory Systems and Their DesignChapter 8 Storage in Mobile Consumer Electronics DevicesChapter 9 Analog Low Pass FiltersChapter 10 Class A AmplifiersChapter 11 MPEG 4 and H 264Chapter 12 Liquid Crystal Displays Hand picked content selected by John Donovan Editor in Chief Portable Design Proven best design practices for low power storage and streamlined development Case histories and design examples get you off and running on your current project

Computer Architecture for Scientists Andrew A. Chien, 2022-03-10 A principled high level view of computer performance and how to exploit it Ideal for software architects and data scientists

Architectural and Operating System Support for Virtual Memory Abhishek Bhattacharjee, Daniel Lustig, 2022-05-31 This book provides computer engineers academic researchers new graduate students and seasoned practitioners an end to end overview of virtual memory We begin with a recap of foundational concepts and discuss not only state of the art virtual memory hardware and software support available today but also emerging research trends in this space The span of topics covers processor microarchitecture memory systems operating system design and memory allocation We show how efficient virtual memory

implementations hinge on careful hardware and software cooperation and we discuss new research directions aimed at addressing emerging problems in this space Virtual memory is a classic computer science abstraction and one of the pillars of the computing revolution It has long enabled hardware flexibility software portability and overall better security to name just a few of its powerful benefits Nearly all user level programs today take for granted that they will have been freed from the burden of physical memory management by the hardware the operating system device drivers and system libraries However despite its ubiquity in systems ranging from warehouse scale datacenters to embedded Internet of Things IoT devices the overheads of virtual memory are becoming a critical performance bottleneck today Virtual memory architectures designed for individual CPUs or even individual cores are in many cases struggling to scale up and scale out to today s systems which now increasingly include exotic hardware accelerators such as GPUs FPGAs or DSPs and emerging memory technologies such as non volatile memory and which run increasingly intensive workloads such as virtualized and or big data applications As such many of the fundamental abstractions and implementation approaches for virtual memory are being augmented extended or entirely rebuilt in order to ensure that virtual memory remains viable and performant in the years to A Primer on Compression in the Memory Hierarchy Somayeh Sardashti, Angelos Arelakis, Per Stenström, David A. Wood, 2022-05-31 This synthesis lecture presents the current state of the art in applying low latency lossless hardware compression algorithms to cache memory and the memory cache link There are many non trivial challenges that must be addressed to make data compression work well in this context First since compressed data must be decompressed before it can be accessed decompression latency ends up on the critical memory access path This imposes a significant constraint on the choice of compression algorithms Second while conventional memory systems store fixed size entities like data types cache blocks and memory pages these entities will suddenly vary in size in a memory system that employs compression Dealing with variable size entities in a memory system using compression has a significant impact on the way caches are organized and how to manage the resources in main memory We systematically discuss solutions in the open literature to these problems Chapter 2 provides the foundations of data compression by first introducing the fundamental concept of value locality We then introduce a taxonomy of compression algorithms and show how previously proposed algorithms fit within that logical framework Chapter 3 discusses the different ways that cache memory systems can employ compression focusing on the trade offs between latency capacity and complexity of alternative ways to compact compressed cache blocks Chapter 4 discusses issues in applying data compression to main memory and Chapter 5 covers techniques for compressing data on the cache to memory links This book should help a skilled memory system designer understand the fundamental challenges in applying compression to the memory hierarchy and introduce him her to the state of the art techniques in addressing them

Attaining High Performance Communications Ada Gavrilovska,2016-04-19 No single solution applied at one particular layer can help applications solve all performance related issues with communication services Instead this book

shows that a coordinated effort is needed among the layers It covers many different types of technologies and layers across the stack from the architectural features of the hardware through the protocols and their implementation in operating system kernels to the manner in which application services and middleware are using underlying platforms. The book also describes key developments in high end platforms high performance interconnection fabrics and communication libraries and multi and Heterogeneous SoC Design and Verification Khaled Salah Mohamed, 2024-03-22 This book covers many core systems the foundations of hardware software codesign on chip communication debugging and verification for heterogenous SoCs Its primary objective is to empower designers in making informed decisions guiding them to strike the perfect balance between flexibility and performance for their SoC designs Readers will benefit from a detailed exploration of the essential elements of the hardware and software codesign framework accompanied by a discussion of the driving motivations behind this approach The author also provides an in depth review of various hardware design architectures shedding light on different design possibilities Furthermore the book presents key concepts concerning hardware and software communication unraveling the intricate interactions within an SoC This book provides a holistic introduction to the methodologies underpinning SoC design and verification making it an indispensable companion for both novice and experienced designers navigating the ever evolving landscape of hardware software codesign Advances in Computer Systems Architecture Chris Jesshope, Colin Egan, 2006-08-29 This book constitutes the refereed proceedings of the 11th Asia Pacific Computer Systems Architecture Conference ACSAC 2006 The book presents 60 revised full papers together with 3 invited lectures addressing such issues as processor and network design reconfigurable computing and operating systems and low level design issues in both hardware and systems Coverage includes large and significant computer based infrastructure projects the challenges of stricter budgets in power dissipation and more A Primer on Memory Persistency Vaibhav Gogte, Aasheesh Kolli, Thomas F. Wenisch, 2022-06-01 This book introduces readers to emerging persistent memory PM technologies that promise the performance of dynamic random access memory DRAM with the durability of traditional storage media such as hard disks and solid state drives SSDs Persistent memories PMs such as Intel's Optane DC persistent memories are commercially available today Unlike traditional storage devices PMs can be accessed over a byte addressable load store interface with access latency that is comparable to DRAM Unfortunately existing hardware and software systems are ill equipped to fully avail the potential of these byte addressable memory technologies as they have been designed to access traditional storage media over a block based interface Several mechanisms have been explored in the research literature over the past decade to design hardware and software systems that provide high performance access to PMs Because PMs are durable they can retain data across failures such as power failures and program crashes Upon a failure recovery mechanisms may inspect PM data reconstruct state and resume program execution Correct recovery of data requires that operations to the PM are properly ordered during normal program execution Memory persistency models define the order in which memory operations

are performed at the PM Much like memory consistency models memory persistency models may be relaxed to improve application performance Several proposals have emerged recently to design memory persistency models for hardware and software systems and for high level programming languages These proposals differ in several key aspects they relax PM ordering constraints introduce varying programmability burden and introduce differing granularity of failure atomicity for PM operations This primer provides a detailed overview of the various classes of the memory persistency models their implementations in hardware programming languages and software systems proposed in the recent research literature and the PM ordering techniques employed by modern processors Digital Design (VHDL) Peter J. Ashenden, 2007-10-24 Digital Design An Embedded Systems Approach Using VHDL provides a foundation in digital design for students in computer engineering electrical engineering and computer science courses It takes an up to date and modern approach of presenting digital logic design as an activity in a larger systems design context Rather than focus on aspects of digital design that have little relevance in a realistic design context this book concentrates on modern and evolving knowledge and design skills Hardware description language HDL based design and verification is emphasized VHDL examples are used extensively throughout By treating digital logic as part of embedded systems design this book provides an understanding of the hardware needed in the analysis and design of systems comprising both hardware and software components Includes a Web site with links to vendor tools labs and tutorials Presents digital logic design as an activity in a larger systems design context Features extensive use of VHDL examples to demonstrate HDL hardware description language usage at the abstract behavioural level and register transfer level as well as for low level verification and verification environments Includes worked examples throughout to enhance the reader s understanding and retention of the material Companion Web site includes links to tools for FPGA design from Synplicity Mentor Graphics and Xilinx VHDL source code for all the examples in the book lecture slides laboratory projects and solutions to exercises A Primer on Memory Consistency and Cache Coherence Daniel Sorin, Mark Hill, David Wood, 2022-11-10 Many modern computer systems and most multicore chips chip multiprocessors support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both highlevel concepts as well as specific concrete examples from real world systems Table of Contents Preface Introduction to Consistency and Coherence Coherence Basics Memory Consistency Motivation and Sequential Consistency Total Store Order and the x86 Memory Model Relaxed Memory Consistency Coherence Protocols

Snooping Coherence Protocols Directory Coherence Protocols Advanced Topics in Coherence Author Biographies Power-Efficient Computer Architectures Magnus Själander, Margaret Martonosi, Stefanos Kaxiras, 2022-05-31 As Moore's Law and Dennard scaling trends have slowed the challenges of building high performance computer architectures while maintaining acceptable power efficiency levels have heightened Over the past ten years architecture techniques for power efficiency have shifted from primarily focusing on module level efficiencies toward more holistic design styles based on parallelism and heterogeneity This work highlights and synthesizes recent techniques and trends in power efficient computer architecture Table of Contents Introduction Voltage and Frequency Management Heterogeneity and Specialization Communication and Memory Systems Conclusions Bibliography Authors Biographies Deep Learning for Computer Architects Brandon Reagen, Robert Adolf, Paul Whatmough, Gu-Yeon Wei, David Brooks, 2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context Multithreading Architecture Mario Nemirovsky, Dean Tullsen, 2022-05-31 Multithreaded architectures now appear across the entire range of computing devices from the highest performing general purpose devices to low end embedded processors Multithreading enables a processor core to more effectively utilize its computational resources as a stall in one thread need not cause execution resources to be idle This enables the computer architect to maximize performance within area constraints power constraints or energy constraints However the architectural options for the processor designer or architect looking to implement multithreading are quite extensive and varied as evidenced not only by the research literature but also by the variety of commercial implementations This book introduces the basic concepts of multithreading describes a number of models of multithreading and then develops

the three classic models coarse grain fine grain and simultaneous multithreading in greater detail It describes a wide variety of architectural and software design tradeoffs as well as opportunities specific to multithreading architectures Finally it details a number of important commercial and academic hardware implementations of multithreading Table of Contents Introduction Multithreaded Execution Models Coarse Grain Multithreading Fine Grain Multithreading Simultaneous Multithreading Managing Contention New Opportunities for Multithreaded Processors Experimentation and Metrics Implementations of Multithreaded Processors Conclusion

Unveiling the Power of Verbal Art: An Emotional Sojourn through The Memory System Bruce Jacob

In a global inundated with screens and the cacophony of fast communication, the profound power and psychological resonance of verbal artistry often diminish in to obscurity, eclipsed by the continuous barrage of sound and distractions. However, situated within the musical pages of **The Memory System Bruce Jacob**, a captivating work of fictional elegance that impulses with organic emotions, lies an unforgettable trip waiting to be embarked upon. Written by a virtuoso wordsmith, this mesmerizing opus books readers on a mental odyssey, delicately exposing the latent possible and profound influence embedded within the intricate internet of language. Within the heart-wrenching expanse of this evocative analysis, we will embark upon an introspective exploration of the book is main subjects, dissect their interesting writing type, and immerse ourselves in the indelible impression it leaves upon the depths of readers souls.

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