

Antonio González · Fernando Latorre  
Grigorios Magklis

# Processor Microarchitecture

An Implementation Perspective



# Processor Microarchitecture An Implementation Perspective Fernando Latorre

**Magnus Själander, Margaret  
Martonosi, Stefanos Kaxiras**





## **Processor Microarchitecture An Implementation Perspective Fernando Latorre:**

*Processor Microarchitecture* Antonio Gonzalez, Fernando Latorre, Grigorios Magklis, 2022-05-31 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies

**Processor Microarchitecture** Antonio González, Fernando Latorre, Grigorios Magklis, 2010-12-30 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate



students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies

Deep Learning for Computer Architects Brandon Reagen,Robert Adolf,Paul Whatmough,Gu-Yeon Wei,David Brooks,2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context

*Power-Efficient Computer Architectures* Magnus Sjölander,Margaret Martonosi,Stefanos Kaxiras,2022-05-31 As Moore s Law and Dennard scaling trends have slowed the challenges of building high performance computer architectures while maintaining acceptable power efficiency levels have heightened Over the past ten years architecture techniques for power efficiency have shifted from primarily focusing on module level efficiencies toward more holistic design styles based on parallelism and heterogeneity This work highlights and synthesizes recent techniques and trends in power efficient computer architecture Table of Contents Introduction Voltage and Frequency Management Heterogeneity and Specialization Communication and Memory Systems Conclusions Bibliography Authors Biographies

**Datacenter Design and Management** Benjamin C. Lee,2022-05-31 An era of big data demands datacenters which house the computing infrastructure that translates raw data into valuable information This book defines datacenters broadly as large distributed systems that perform parallel computation for diverse users These systems exist in multiple forms private and public and are built at multiple scales Datacenter design and management is multifaceted requiring the simultaneous pursuit of multiple objectives Performance



efficiency and fairness are first order design and management objectives which can each be viewed from several perspectives This book surveys datacenter research from a computer architect s perspective addressing challenges in applications design management server simulation and system simulation This perspective complements the rich bodies of work in datacenters as a warehouse scale system which study the implications for infrastructure that encloses computing equipment and in datacenters as distributed systems which employ abstract details in processor and memory subsystems This book is written for first or second year graduate students in computer architecture and may be helpful for those in computer systems The goal of this book is to prepare computer architects for datacenter oriented research by describing prevalent perspectives and the state of the art

*Quantum Computer Systems* Yongshan Ding, Frederic T. Chong, 2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing

*Deep Learning Systems* Andres Rodriguez, 2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in



industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to better collaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book

### **AI for Computer**

**Architecture** Lizhong Chen,Drew Penney,Daniel Jiménez,2022-05-31 Artificial intelligence has already enabled pivotal advances in diverse fields yet its impact on computer architecture has only just begun In particular recent work has explored broader application to the design optimization and simulation of computer architecture Notably machine learning based strategies often surpass prior state of the art analytical heuristic and human expert approaches This book reviews the application of machine learning in system wide simulation and run time optimization and in many individual components such as caches memories branch predictors networks on chip and GPUs The book further analyzes current practice to highlight useful design strategies and identify areas for future work based on optimized implementation strategies opportune extensions to existing work and ambitious long term possibilities Taken together these strategies and techniques present a promising future for increasingly automated computer architecture designs

### **Optimization and Mathematical**

**Modeling in Computer Architecture** Karthikeyan Sankaralingam,Michael Ferris,Tony Nowatzki,Cristian Estan,Nilay Vaish,David Wood,2022-05-31 In this book we give an overview of modeling techniques used to describe computer systems to mathematical optimization tools We give a brief introduction to various classes of mathematical optimization frameworks with special focus on mixed integer linear programming which provides a good balance between solver time and expressiveness We present four detailed case studies instruction set customization data center resource management spatial architecture scheduling and resource allocation in tiled architectures showing how MILP can be used and quantifying by how much it outperforms traditional design exploration techniques This book should help a skilled systems designer to learn techniques for using MILP in their problems and the skilled optimization expert to understand the types of computer systems problems that MILP can be applied to

### **A Primer on Hardware Prefetching** Babak Falsafi,Thomas F. Wenisch,2022-06-01

Since the 1970 s microprocessor based digital platforms have been riding Moore s law allowing for doubling of density for the same area roughly every two years However whereas microprocessor fabrication has focused on increasing instruction



execution rate memory fabrication technologies have focused primarily on an increase in capacity with negligible increase in speed This divergent trend in performance between the processors and memory has led to a phenomenon referred to as the Memory Wall To overcome the memory wall designers have resorted to a hierarchy of cache memory levels which rely on the principal of memory access locality to reduce the observed memory access time and the performance gap between processors and memory Unfortunately important workload classes exhibit adverse memory access patterns that baffle the simple policies built into modern cache hierarchies to move instructions and data across cache levels As such processors often spend much time idling upon a demand fetch of memory blocks that miss in higher cache levels Prefetching predicting future memory accesses and issuing requests for the corresponding memory blocks in advance of explicit accesses is an effective approach to hide memory access latency There have been a myriad of proposed prefetching techniques and nearly every modern processor includes some hardware prefetching mechanisms targeting simple and regular memory access patterns This primer offers an overview of the various classes of hardware prefetchers for instructions and data proposed in the research literature and presents examples of techniques incorporated into modern microprocessors

Space-Time Computing with Temporal Neural Networks James E. Smith, 2022-05-31 Understanding and implementing the brain's computational paradigm is the one true grand challenge facing computer researchers Not only are the brain's computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain's computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain's neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing study and progress to date is described in detail in later chapters Simulation plays a



major role in model development and the simulation infrastructure developed by the author is described

**Automatic Parallelization** Samuel Midkiff, 2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading Single-Instruction Multiple-Data Execution Christopher J. Hughes, 2022-05-31 Having hit power limitations to even more aggressive out of order execution in processor cores many architects in the past decade have turned to single instruction multiple data SIMD execution to increase single threaded performance SIMD execution or having a single instruction drive execution of an identical operation on multiple data items was already well established as a technique to efficiently exploit data parallelism Furthermore support for it was already included in many commodity processors However in the past decade SIMD execution has seen a dramatic increase in the set of applications using it which has motivated big improvements in hardware support in mainstream microprocessors The easiest way to provide a big performance boost to SIMD hardware is to make it wider i e increase the number of data items hardware operates on simultaneously Indeed microprocessor vendors have done this However as we exploit more data parallelism in applications certain challenges can negatively impact performance In particular conditional execution non contiguous memory accesses and the presence of some dependences across data items are key roadblocks to achieving peak performance with SIMD execution This book first describes data parallelism and why it is so common in popular applications We then describe SIMD execution and explain where its performance and energy benefits come from compared to other techniques to exploit parallelism Finally we describe SIMD hardware support in current commodity microprocessors This includes both expected design tradeoffs as well as unexpected ones as we work to overcome challenges encountered when trying to map real software to SIMD execution Customizable Computing Yu-Ting Chen, Jason Cong, Michael Gill, Glenn Reinman, Bingjun Xiao, 2022-05-31 Since the end of Dennard scaling in the early 2000s improving the energy efficiency of computation has been the main concern of the research community and industry The large energy efficiency gap between



general purpose processors and application specific integrated circuits ASICs motivates the exploration of customizable architectures where one can adapt the architecture to the workload In this Synthesis lecture we present an overview and introduction of the recent developments on energy efficient customizable architectures including customizable cores and accelerators on chip memory customization and interconnect optimization In addition to a discussion of the general techniques and classification of different approaches used in each area we also highlight and illustrate some of the most successful design examples in each category and discuss their impact on performance and energy efficiency We hope that this work captures the state of the art research and development on customizable architectures and serves as a useful reference basis for further research design and implementation for large scale deployment in future computing systems

**Data Orchestration in Deep Learning Accelerators** Tushar Krishna, Hyoukjun Kwon, Angshuman Parashar, Michael Pellauer, Ananda Samajdar, 2022-05-31 This Synthesis Lecture focuses on techniques for efficient data orchestration within DNN accelerators The End of Moore's Law coupled with the increasing growth in deep learning and other AI applications has led to the emergence of custom Deep Neural Network DNN accelerators for energy efficient inference on edge devices Modern DNNs have millions of hyper parameters and involve billions of computations this necessitates extensive data movement from memory to on chip processing engines It is well known that the cost of data movement today surpasses the cost of the actual computation therefore DNN accelerators require careful orchestration of data across on chip compute network and memory elements to minimize the number of accesses to external DRAM The book covers DNN dataflows data reuse buffer hierarchies networks on chip and automated design space exploration It concludes with data orchestration challenges with compressed and sparse DNNs and future trends The target audience is students engineers and researchers interested in designing high performance and low energy accelerators for DNN inference [A Primer on Memory](#)

[Consistency and Cache Coherence, Second Edition](#) Vijay Nagarajan, Daniel J. Sorin, Mark D. Hill, David A. Wood, 2022-05-31 Many modern computer systems including homogeneous and heterogeneous architectures support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both high level concepts as well as specific concrete examples from real world systems This second edition reflects a decade of advancements since the first edition and includes among other more modest changes two new chapters one on consistency and coherence for non CPU accelerators with a focus on GPUs and one that points to formal work and



tools on consistency and coherence

### **Quantum Computing for Computer Architects, Second Edition** Tzvetan

Metodi, Arvin I. Faruque, 2022-06-01 Quantum computers can in theory solve certain problems far faster than a classical computer running any known classical algorithm While existing technologies for building quantum computers are in their infancy it is not too early to consider their scalability and reliability in the context of the design of large scale quantum computers To architect such systems one must understand what it takes to design and model a balanced fault tolerant quantum computer architecture The goal of this lecture is to provide architectural abstractions for the design of a quantum computer and to explore the systems level challenges in achieving scalable fault tolerant quantum computation In this lecture we provide an engineering oriented introduction to quantum computation with an overview of the theory behind key quantum algorithms Next we look at architectural case studies based upon experimental data and future projections for quantum computation implemented using trapped ions While we focus here on architectures targeted for realization using trapped ions the techniques for quantum computer architecture design quantum fault tolerance and compilation described in this lecture are applicable to many other physical technologies that may be viable candidates for building a large scale quantum computing system We also discuss general issues involved with programming a quantum computer as well as a discussion of work on quantum architectures based on quantum teleportation Finally we consider some of the open issues remaining in the design of quantum computers Table of Contents Introduction Basic Elements for Quantum Computation Key Quantum Algorithms Building Reliable and Scalable Quantum Architectures Simulation of Quantum Computation Architectural Elements Case Study The Quantum Logic Array Architecture Programming the Quantum Architecture Using the QLA for Quantum Simulation The Transverse Ising Model Teleportation Based Quantum Architectures Concluding Remarks

*Hardware and Software Support for Virtualization* Edouard Bugnion, Jason Nieh, Dan Tsafir, 2022-06-01 This book focuses on the core question of the necessary architectural support provided by hardware to efficiently run virtual machines and of the corresponding design of the hypervisors that run them Virtualization is still possible when the instruction set architecture lacks such support but the hypervisor remains more complex and must rely on additional techniques Despite the focus on architectural support in current architectures some historical perspective is necessary to appropriately frame the problem The first half of the book provides the historical perspective of the theoretical framework developed four decades ago by Popek and Goldberg It also describes earlier systems that enabled virtualization despite the lack of architectural support in hardware As is often the case theory defines a necessary but not sufficient set of features and modern architectures are the result of the combination of the theoretical framework with insights derived from practical systems The second half of the book describes state of the art support for virtualization in both x86 64 and ARM processors This book includes an in depth description of the CPU memory and I O virtualization of these two processor architectures as well as case studies on the Linux KVM VMware and Xen hypervisors It concludes with a performance comparison of



virtualization on current generation x86 and ARM based systems across multiple hypervisors      **Innovations in the Memory System** Rajeev Balasubramonian, 2022-05-31 The memory system has the potential to be a hub for future innovation While conventional memory systems focused primarily on high density other memory system metrics like energy security and reliability are grabbing modern research headlines With processor performance stagnating it is also time to consider new programming models that move some application computations into the memory system This in turn will lead to feature rich memory systems with new interfaces The past decade has seen a number of memory system innovations that point to this future where the memory system will be much more than dense rows of unintelligent bits This book takes a tour through recent and prominent research works touching upon new DRAM chip designs and technologies near data processing approaches new memory channel architectures techniques to tolerate the overheads of refresh and fault tolerance security attacks and mitigations and memory scheduling      *Resilient Architecture Design for Voltage Variation* Vijay Janapa Reddi, Meeta Sharma Gupta, 2022-05-31 Shrinking feature size and diminishing supply voltage are making circuits sensitive to supply voltage fluctuations within the microprocessor caused by normal workload activity changes If left unattended voltage fluctuations can lead to timing violations or even transistor lifetime issues that degrade processor robustness Mechanisms that learn to tolerate avoid and eliminate voltage fluctuations based on program and microarchitectural events can help steer the processor clear of danger thus enabling tighter voltage margins that improve performance or lower power consumption We describe the problem of voltage variation and the factors that influence this variation during processor design and operation We also describe a variety of runtime hardware and software mitigation techniques that either tolerate avoid and or eliminate voltage violations We hope processor architects will find the information useful since tolerance avoidance and elimination are generalizable constructs that can serve as a basis for addressing other reliability challenges as well Table of Contents Introduction Modeling Voltage Variation Understanding the Characteristics of Voltage Variation Traditional Solutions and Emerging Solution Forecast Allowing and Tolerating Voltage Emergencies Predicting and Avoiding Voltage Emergencies Eliminating Recurring Voltage Emergencies Future Directions on Resiliency



Delve into the emotional tapestry woven by in Experience **Processor Microarchitecture An Implementation Perspective Fernando Latorre** . This ebook, available for download in a PDF format ( Download in PDF: \*), is more than just words on a page; itis a journey of connection and profound emotion. Immerse yourself in narratives that tug at your heartstrings. Download now to experience the pulse of each page and let your emotions run wild.

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#### **Processor Microarchitecture An Implementation Perspective Fernando Latorre Introduction**

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