
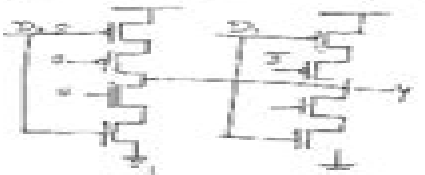



**Model Question Paper with effect from 2022-23 (CBCS Scheme)**  
**Sixth Semester B.E. Degree Examination**  
**VLSI Design and Testing (21EC63)**  
**ANSWERS**

Q. No	Answers	Marks															
1 a	<p>With necessary circuit diagram explain the operation of tristate inverter. Also realize 2:1 mux using tristate inverter.</p> <p><u>Tristate Inverter</u></p>  <p><u>Truth Table</u></p> <table border="1"> <thead> <tr> <th>BM</th> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>x</td> </tr> <tr> <td>0</td> <td>1</td> <td>x</td> </tr> </tbody> </table> <p>(4m)</p> <p><u>2:1 Multiplexer using tristate inverter</u></p>  <p>(4m)</p>	BM	A	Y	1	0	1	1	1	0	0	0	x	0	1	x	
BM	A	Y															
1	0	1															
1	1	0															
0	0	x															
0	1	x															
B	<p>Realize the CMOS gate for the following function <math>Y = A(B+C) + DE</math></p> <p><u>Realization of CMOS gate for <math>Y = A(B+C) + DE</math></u></p> <p><u>Full-down network</u></p> <p><math>A(B+C) + DE</math>  <math>\overline{A(B+C) + DE}</math>  <math>\overline{A(B+C)} \cdot \overline{DE}</math>  <math>(\overline{A} + \overline{B} + \overline{C}) \cdot (\overline{D} + \overline{E})</math>  <math>(\overline{A} + \overline{B} + \overline{C}) \cdot (\overline{D} + \overline{E})</math></p> <p><u>Full-up network</u></p> <p><math>A(B+C) + DE</math>  <math>A(B+C) + DE</math>  <math>A(B+C) + DE</math>  <math>A(B+C) + DE</math></p> <p><u>CMOS Gate</u></p>  <p>(10m)</p>																

# Vlsi Design Sixth Sem Question Paper

**Yijin Wang**



## Vlsi Design Sixth Sem Question Paper:

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