Quantum Computing for Computer Architects

Second Edition

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Quantum Computing For Computer Architects Frederic T Chong

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Quantum Computing for Computer Architects Tzvetan S. Metodi,Arvin I. Faruque,Frederic T. Chong,2011 Quantum computation may seem to be a topic for science fiction but small quantum computers have existed for several years and larger machines are on the drawing table These efforts have been fueled by a tantalizing property while conventional computers employ a binary representation that allows computational power to scale linearly with resources at best quantum computations employ quantum phenomena that can interact to allow computational power that is exponential in the number of quantum bits in the system Quantum devices rely on the ability to control and manipulate binary data stored in the phase information of quantum wave functions that describe the electronic states of individual atoms or the polarization states of photons While existing quantum technologies are in their infancy we shall see that it is not too early to consider scalability and reliability In fact such considerations are a critical link in the development chain of viable device technologies capable of orchestrating reliable control of tens of millions quantum bits in a large scale system The goal of this lecture is to provide architectural abstractions common to potential technologies and explore the systems level challenges in achieving scalable fault tolerant quantum computation   *Quantum Computing for Computer Architects, Second Edition* Tzvetan Metodi,Arvin I. Faruque,2022-06-01 Quantum computers can in theory solve certain problems far faster than a classical computer running any known classical algorithm While existing technologies for building quantum computers are in their infancy it is not too early to consider their scalability and reliability in the context of the design of large scale quantum computers To architect such systems one must understand what it takes to design and model a balanced fault tolerant quantum computer architecture The goal of this lecture is to provide architectural abstractions for the design of a quantum computer and to explore the systems level challenges in achieving scalable fault tolerant quantum computation In this lecture we provide an engineering oriented introduction to quantum computation with an overview of the theory behind key quantum algorithms Next we look at architectural case studies based upon experimental data and future projections for quantum computation implemented using trapped ions While we focus here on architectures targeted for realization using trapped ions the techniques for quantum computer architecture design quantum fault tolerance and compilation described in this lecture are applicable to many other physical technologies that may be viable candidates for building a large scale quantum computing system We also discuss general issues involved with programming a quantum computer as well as a discussion of work on quantum architectures based on quantum teleportation Finally we consider some of the open issues remaining in the design of quantum computers Table of Contents Introduction Basic Elements for Quantum Computation Key Quantum Algorithms Building Reliable and Scalable Quantum Architectures Simulation of Quantum Computation Architectural Elements Case Study The Quantum Logic Array Architecture Programming the Quantum Architecture Using the QLA for Quantum Simulation The Transverse Ising Model Teleportation Based Quantum Architectures Concluding Remarks   **Quantum**

Computing for Computer Architects Tzvetan S. Metodi,Frederic T. Chong,2022-12-06 Quantum computation may seem to be a topic for science fiction but small quantum computers have existed for several years and larger machines are on the drawing table These efforts have been fueled by a tantalizing property while conventional computers employ a binary representation that allows computational power to scale linearly with resources at best quantum computations employ quantum phenomena that can interact to allow computational power that is exponential in the number of quantum bits in the system Quantum devices rely on the ability to control and manipulate binary data stored in the phase information of quantum wave functions that describe the electronic states of individual atoms or the polarization states of photons While existing quantum technologies are in their infancy we shall see that it is not too early to consider scalability and reliability In fact such considerations are a critical link in the development chain of viable device technologies capable oforchestrating reliable control of tens of millions quantum bits in a large scale system The goal of this lecture is to provide architectural abstractions common to potential technologies and explore the systemslevel challenges in achieving scalable fault tolerant quantum computation The central premise of the lecture is directed at quantum computation QC architectural issues We stress the fact that the basic tenet of large scale quantum computing is reliability through system balance the need to protect and control the quantum information just long enough for the algorithm to complete execution To architectQCsystems onemust understand what it takes to design and model a balanced fault tolerant quantum architecture just as the concept of balance drives conventional architectural design For example the register file depth in classical computers is matched to the number of functional units the memory bandwidth to the cache miss rate or the interconnect bandwidth matched to the compute power of each element of a multiprocessor We provide an engineering oriented introduction to quantum computation and provide an architectural case study based upon experimental data and future projection for ion trap technology We apply the concept of balance to the design of a quantum computer creating an architecture model that balances both quantum and classical resources in terms of exploitable parallelism in quantum applications From this framework we also discuss the many open issues remaining in designing systems to perform quantum computation *Synthesis Lectures on Computer Architecture : Quantum Computing for Computer Architects (2nd Edition)* Tzvetan S. Metodi, **Computer Architecture** Joseph D. Dumas II,2018-10-03 Future computing professionals must become familiar with historical computer architectures because many of the same or similar techniques are still being used and may persist well into the future Computer Architecture Fundamentals and Principles of Computer Design discusses the fundamental principles of computer design and performance enhancement that have proven effective and demonstrates how current trends in architecture and implementation rely on these principles while expanding upon them or applying them in new ways Rather than focusing on a particular type of machine this textbook explains concepts and techniques via examples drawn from various architectures and implementations When necessary the author creates simplified examples that clearly explain architectural and

implementation features used across many computing platforms Following an introduction that discusses the difference between architecture and implementation and how they relate the next four chapters cover the architecture of traditional single processor systems that are still after 60 years the most widely used computing machines The final two chapters explore approaches to adopt when single processor systems do not reach desired levels of performance or are not suited for intended applications Topics include parallel systems major classifications of architectures and characteristics of unconventional systems of the past present and future This textbook provides students with a thorough grounding in what constitutes high performance and how to measure it as well as a full familiarity in the fundamentals needed to make systems perform better This knowledge enables them to understand and evaluate the many new systems they will encounter throughout their professional careers **Quantum Computer Systems** Yongshan Ding,Frederic T. Chong,2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing **AI for Computer Architecture** Lizhong Chen,Drew Penney,Daniel Jiménez,2022-05-31 Artificial intelligence has already enabled pivotal advances in diverse fields yet its impact on computer architecture has only just begun In particular recent work has explored broader application to the design optimization and simulation of computer architecture Notably machine learning based strategies often surpass prior state of the art analytical heuristic and human expert approaches This book reviews the application of machine learning in system wide simulation and run time optimization and in many individual components such as caches memories branch predictors networks on chip and GPUs The book further analyzes current practice to highlight useful design strategies and identify areas for future work based on optimized implementation strategies opportune extensions to existing work and ambitious long term possibilities Taken together these strategies and techniques present a promising future for increasingly automated computer architecture designs Optimization and Mathematical Modeling in Computer Architecture Karthikeyan Sankaralingam,Michael Ferris,Tony Nowatzki,Cristian Estan,Nilay Vaish,David Wood,2022-05-31 In this book we give an overview of modeling techniques used to describe computer systems to mathematical optimization tools We give a brief introduction to various classes of mathematical optimization frameworks with special focus on mixed integer linear programming which provides a

good balance between solver time and expressiveness We present four detailed case studies instruction set customization data center resource management spatial architecture scheduling and resource allocation in tiled architectures showing how MILP can be used and quantifying by how much it outperforms traditional design exploration techniques This book should help a skilled systems designer to learn techniques for using MILP in their problems and the skilled optimization expert to understand the types of computer systems problems that MILP can be applied to <u>The Datacenter as a Computer</u> Luiz Barroso,Urs Hoelzle,2022-11-10 As computation continues to move into the cloud the computing platform of interest no longer resembles a pizza box or a refrigerator but a warehouse full of computers These new large datacenters are quite different from traditional hosting facilities of earlier times and cannot be viewed simply as a collection of co located servers Large portions of the hardware and software resources in these facilities must work in concert to efficiently deliver good levels of Internet service performance something that can only be achieved by a holistic approach to their design and deployment In other words we must treat the datacenter itself as one massive warehouse scale computer WSC We describe the architecture of WSCs the main factors influencing their design operation and cost structure and the characteristics of their software base We hope it will be useful to architects and programmers of today s WSCs as well as those of future many core platforms which may one day implement the equivalent of today s WSCs on a single board Table of Contents Introduction Workloads and Software Infrastructure Hardware Building Blocks Datacenter Basics Energy and Power Efficiency Modeling Costs Dealing with Failures and Repairs Closing Remarks *Computer Architecture Techniques for Power-Efficiency* Stefanos Kaxiras,Margaret Martonosi,2022-06-01 In the last few years power dissipation has become an important design constraint on par with performance in the design of new computer systems Whereas in the past the primary job of the computer architect was to translate improvements in operating frequency and transistor count into performance now power efficiency must be taken into account at every step of the design process While for some time architects have been successful in delivering 40% to 50% annual improvement in processor performance costs that were previously brushed aside eventually caught up The most critical of these costs is the inexorable increase in power dissipation and power density in processors Power dissipation issues have catalyzed new topic areas in computer architecture resulting in a substantial body of work on more power efficient architectures Power dissipation coupled with diminishing performance gains was also the main cause for the switch from single core to multi core architectures and a slowdown in frequency increase This book aims to document some of the most important architectural techniques that were invented proposed and applied to reduce both dynamic power and static power dissipation in processors and memory hierarchies A significant number of techniques have been proposed for a wide range of situations and this book synthesizes those techniques by focusing on their common characteristics Table of Contents Introduction Modeling Simulation and Measurement Using Voltage and Frequency Adjustments to Manage Dynamic Power Optimizing Capacitance and Switching Activity to Reduce Dynamic Power Managing

Static Leakage Power Conclusions *Fault Tolerant Computer Architecture* Daniel Sorin,2022-05-31 For many years most computer architects have pursued one primary goal performance Architects have translated the ever increasing abundance of ever faster transistors provided by Moore s law into remarkable increases in performance Recently however the bounty provided by Moore s law has been accompanied by several challenges that have arisen as devices have become smaller including a decrease in dependability due to physical faults In this book we focus on the dependability challenge and the fault tolerance solutions that architects are developing to overcome it The two main purposes of this book are to explore the key ideas in fault tolerant computer architecture and to present the current state of the art over approximately the past 10 years in academia and industry Table of Contents Introduction Error Detection Error Recovery Diagnosis Self Repair The Future Deep Learning for Computer Architects Brandon Reagen,Robert Adolf,Paul Whatmough,Gu-Yeon Wei,David Brooks,2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context Innovations in the Memory System Rajeev Balasubramonian,2022-05-31 The memory system has the potential to be a hub for future innovation While conventional memory systems focused primarily on high density other memory system metrics like energy security and reliability are grabbing modern research headlines With processor performance stagnating it is also time to consider new programming models that move some application computations into the memory system This in turn will lead to feature rich memory systems with new interfaces The past decade has seen a number of memory system innovations that point to this future where the memory system will be much more than dense rows of unintelligent bits This book takes a tour through recent and prominent research works touching upon new DRAM chip designs and technologies near data processing

approaches new memory channel architectures techniques to tolerate the overheads of refresh and fault tolerance security attacks and mitigations and memory scheduling *A Primer on Memory Persistency* Vaibhav Gogte,Aasheesh Kolli,Thomas F. Wenisch,2022-06-01 This book introduces readers to emerging persistent memory PM technologies that promise the performance of dynamic random access memory DRAM with the durability of traditional storage media such as hard disks and solid state drives SSDs Persistent memories PMs such as Intel s Optane DC persistent memories are commercially available today Unlike traditional storage devices PMs can be accessed over a byte addressable load store interface with access latency that is comparable to DRAM Unfortunately existing hardware and software systems are ill equipped to fully avail the potential of these byte addressable memory technologies as they have been designed to access traditional storage media over a block based interface Several mechanisms have been explored in the research literature over the past decade to design hardware and software systems that provide high performance access to PMs Because PMs are durable they can retain data across failures such as power failures and program crashes Upon a failure recovery mechanisms may inspect PM data reconstruct state and resume program execution Correct recovery of data requires that operations to the PM are properly ordered during normal program execution Memory persistency models define the order in which memory operations are performed at the PM Much like memory consistency models memory persistency models may be relaxed to improve application performance Several proposals have emerged recently to design memory persistency models for hardware and software systems and for high level programming languages These proposals differ in several key aspects they relax PM ordering constraints introduce varying programmability burden and introduce differing granularity of failure atomicity for PM operations This primer provides a detailed overview of the various classes of the memory persistency models their implementations in hardware programming languages and software systems proposed in the recent research literature and the PM ordering techniques employed by modern processors **High Performance Datacenter Networks** Dennis Abts,John Kim,2022-05-31 Datacenter networks provide the communication substrate for large parallel computer systems that form the ecosystem for high performance computing HPC systems and modern Internet applications The design of new datacenter networks is motivated by an array of applications ranging from communication intensive climatology complex material simulations and molecular dynamics to such Internet applications as Web search language translation collaborative Internet applications streaming video and voice over IP For both Supercomputing and Cloud Computing the network enables distributed applications to communicate and interoperate in an orchestrated and efficient way This book describes the design and engineering tradeoffs of datacenter networks It describes interconnection networks from topology and network architecture to routing algorithms and presents opportunities for taking advantage of the emerging technology trends that are influencing router microarchitecture With the emergence of many core processor chips it is evident that we will also need many port routing chips to provide a bandwidth rich network to avoid the performance limiting effects of Amdahl s Law

We provide an overview of conventional topologies and their routing algorithms and show how technology signaling rates and cost effective optics are motivating new network topologies that scale up to millions of hosts The book also provides detailed case studies of two high performance parallel computer systems and their networks Table of Contents Introduction Background Topology Basics High Radix Topologies Routing Scalable Switch Microarchitecture System Packaging Case Studies Closing Remarks **Processor Microarchitecture** Antonio Gonzalez,Fernando Latorre,Grigorios Magklis,2022-05-31 This lecture presents a study of the microarchitecture of contemporary microprocessors The focus is on implementation aspects with discussions on their implications in terms of performance power and cost of state of the art designs The lecture starts with an overview of the different types of microprocessors and a review of the microarchitecture of cache memories Then it describes the implementation of the fetch unit where special emphasis is made on the required support for branch prediction The next section is devoted to instruction decode with special focus on the particular support to decoding x86 instructions The next chapter presents the allocation stage and pays special attention to the implementation of register renaming Afterward the issue stage is studied Here the logic to implement out of order issue for both memory and non memory instructions is thoroughly described The following chapter focuses on the instruction execution and describes the different functional units that can be found in contemporary microprocessors as well as the implementation of the bypass network which has an important impact on the performance Finally the lecture concludes with the commit stage where it describes how the architectural state is updated and recovered in case of exceptions or misspeculations This lecture is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture It is also intended for practitioners in the industry in the area of microprocessor design The book assumes that the reader is familiar with the main concepts regarding pipelining out of order execution cache memories and virtual memory Table of Contents Introduction Caches The Instruction Fetch Unit Decode Allocation The Issue Stage Execute The Commit Stage References Author Biographies **A Primer on Compression in the Memory Hierarchy** Somayeh Sardashti,Angelos Arelakis,Per Stenström,David A. Wood,2022-05-31 This synthesis lecture presents the current state of the art in applying low latency lossless hardware compression algorithms to cache memory and the memory cache link There are many non trivial challenges that must be addressed to make data compression work well in this context First since compressed data must be decompressed before it can be accessed decompression latency ends up on the critical memory access path This imposes a significant constraint on the choice of compression algorithms Second while conventional memory systems store fixed size entities like data types cache blocks and memory pages these entities will suddenly vary in size in a memory system that employs compression Dealing with variable size entities in a memory system using compression has a significant impact on the way caches are organized and how to manage the resources in main memory We systematically discuss solutions in the open literature to these problems Chapter 2

provides the foundations of data compression by first introducing the fundamental concept of value locality We then introduce a taxonomy of compression algorithms and show how previously proposed algorithms fit within that logical framework Chapter 3 discusses the different ways that cache memory systems can employ compression focusing on the trade offs between latency capacity and complexity of alternative ways to compact compressed cache blocks Chapter 4 discusses issues in applying data compression to main memory and Chapter 5 covers techniques for compressing data on the cache to memory links This book should help a skilled memory system designer understand the fundamental challenges in applying compression to the memory hierarchy and introduce him her to the state of the art techniques in addressing them

Dynamic Binary Modification Kim Hazelwood,2022-05-31 Dynamic binary modification tools form a software layer between a running application and the underlying operating system providing the powerful opportunity to inspect and potentially modify every user level guest application instruction that executes Toolkits built upon this technology have enabled computer architects to build powerful simulators and emulators for design space exploration compiler writers to analyze and debug the code generated by their compilers software developers to fully explore the features bottlenecks and performance of their software and even end users to extend the functionality of proprietary software running on their computers Several dynamic binary modification systems are freely available today that place this power into the hands of the end user While these systems are quite complex internally they mask that complexity with an easy to learn API that allows a typical user to ramp up fairly quickly and build any of a number of powerful tools Meanwhile these tools are robust enough to form the foundation for software products in use today This book serves as a primer for researchers interested in dynamic binary modification systems their internal design structure and the wide range of tools that can be built leveraging these systems The hands on examples presented throughout form a solid foundation for designing and constructing more complex tools with an appreciation for the techniques necessary to make those tools robust and efficient Meanwhile the reader will get an appreciation for the internal design of the engines themselves Table of Contents Dynamic Binary Modification Overview Using a Dynamic Binary Modifier Program Analysis and Debugging Active Program Modification Architectural Exploration Advanced System Internals Historical Perspectives Summary and Observations   Automatic Parallelization Samuel Midkiff,2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude

with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading   Phase Change Memory Naveen Muralimanohar,Moinuddin K. Qureshi,Sudhanva Gurumurthi,Bipin Rajendran,2022-05-31 As conventional memory technologies such as DRAM and Flash run into scaling challenges architects and system designers are forced to look at alternative technologies for building future computer systems This synthesis lecture begins by listing the requirements for a next generation memory technology and briefly surveys the landscape of novel non volatile memories Among these Phase Change Memory PCM is emerging as a leading contender and the authors discuss the material device and circuit advances underlying this exciting technology The lecture then describes architectural solutions to enable PCM for main memories Finally the authors explore the impact of such byte addressable non volatile memories on future storage and system designs Table of Contents Next Generation Memory Technologies Architecting PCM for Main Memories Tolerating Slow Writes in PCM Wear Leveling for Durability Wear Leveling Under Adversarial Settings Error Resilience in Phase Change Memories Storage and System Design With Emerging Non Volatile Memories

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