

## Code Coverage Management - Testplan

Testplan: C:\Program Files\Microsoft Visual Studio\VC98\WinSxS\Code Coverage Management - Testplan

Testplan Section / Coverage Unit	Type	Coverage	Status	Goal	% of Goal	Weight	Link Status	Sec #	Brn	Wts	% Wt
Testplan	Testplan	88.24%		-	88.24%	1	Partial	0	1248	4392	81.82%
Coverage Plan	Testplan	88.89%		100%	88.89%	1	Partial	1	1716	4392	81.82%
Testplan	Testplan	87.71%		100%	87.71%	1	Partial	1.1	1412	1648	74.18%
Preprocessor	Testplan	81.25%		100%	81.25%	1	Open	1.2	16	7	79%
Post-processor	Testplan	68.95%		100%	68.95%	1	Open	1.3	26	14	65.45%
Frame, State, Arbitrator	Testplan	100%		100%	100%	1	Open	1.4	8	8	100%
Microprocessor Interface	Testplan	75.4%		100%	75.4%	1	Open	1.5	516	685	75.33%
All Code Coverage	Testplan	88.53%		100%	88.53%	1	Open	1.6	1267	2912	87.99%
Toggle Coverage	Testplan	67.21%		100%	67.21%	1	Open	1.6.1	1	8	8%
FPM Coverage	Testplan	88.20%		100%	88.20%	1	Open	1.6.2	62	55	88.7%
Branch Coverage	Testplan	81.81%		100%	81.81%	1	Open	1.6.3	1826	1747	88.7%
Condition Coverage	Testplan	67.83%		100%	67.83%	1	Open	1.6.4	642	648	99.1%
Expression Coverage	Testplan	67.8%		100%	67.8%	1	Open	1.6.5	475	281	69.75%
Statement Coverage	Testplan	95%		100%	95%	1	Open	1.6.6	1	6	8%
All Assertions	Testplan	18.88%		100%	18.88%	1	Open	1.7	12	7	18.88%
Functional Coverage Example	Testplan	62.5%		100%	62.5%	1	Open	1.8	8	5	62.5%
coverage_01	Testplan	62.5%		100%	62.5%	1	Open	1.8.1	8	5	62.5%
01_FPM_01	Testplan	75%		100%	75%	1	Open	1.8...	8	3	75%
coverage_02_01	Testplan	100%		100%	100%	1	Open	1.8...	2	2	100%
Assert_tester_output_01_01_01_01	CoverPlan	100%		100%	100%	1			2	2	100%
Assert_tester_output_01_01_01_01_01	Cov Brn	100%		-	100%	1			1	1	100%
Assert_tester_output_01_01_01_01_01_01	Cov Brn	100%		-	100%	1			1	1	100%
coverage_03_01	Testplan	50%		100%	50%	1	Open	1.8...	2	1	50%
01_FPM_02	Testplan	50%		100%	50%	1	Open	1.8...	8	2	50%
Test Plan	Testplan	75%		100%	75%	1	Open	2	14	11	78.57%

# Questasim User Manual

**Joel Grodstein**



## Questasim User Manual:

**Synthesizable VHDL Design for FPGAs** Eduardo Augusto Bezerra,Djones Vinicius Lettnin,2013-10-21 The methodology described in this book is the result of many years of research experience in the field of synthesizable VHDL design targeting FPGA based platforms VHDL was first conceived as a documentation language for ASIC designs Afterwards the language was used for the behavioral simulation of ASICs and also as a design input for synthesis tools VHDL is a rich language but just a small subset of it can be used to write synthesizable code from which a physical circuit can be obtained Usually VHDL books describe both synthesis and simulation aspects of the language but in this book the reader is conducted just through the features acceptable by synthesis tools The book introduces the subjects in a gradual and concise way providing just enough information for the reader to develop their synthesizable digital systems in VHDL The examples in the book were planned targeting an FPGA platform widely used around the world [A Practical Approach to VLSI System on Chip \(SoC\) Design](#) Veena S. Chakravarthi,2022-12-13 Now in a thoroughly revised second edition this practical practitioner guide provides a comprehensive overview of the SoC design process It explains end to end system on chip SoC design processes and includes updated coverage of design methodology the design environment EDA tool flow design decisions choice of design intellectual property IP cores sign off procedures and design infrastructure requirements The second edition provides new information on SOC trends and updated design cases Coverage also includes critical advanced guidance on the latest UPF based low power design flow challenges of deep submicron technologies and 3D design fundamentals which will prepare the readers for the challenges of working at the nanotechnology scale [A Practical Approach to VLSI System on Chip SoC Design A Comprehensive Guide Second Edition](#) provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools It will be a valuable professional reference for those working on VLSI design and verification portfolios in complex SoC designs **Digital VLSI Design with Verilog** John Michael Williams,2014-06-17 This book is structured as a step by step course of study along the lines of a VLSI integrated circuit design project The entire Verilog language is presented from the basics to everything necessary for synthesis of an entire 70 000 transistor full duplex serializer deserializer including synthesizable PLLs The author includes everything an engineer needs for in depth understanding of the Verilog language Syntax semantics simulation and test Complete solutions for the 27 labs are provided in the downloadable files that accompany the book For readers with access to appropriate electronic design tools all solutions can be developed simulated and synthesized as described in the book A partial list of design topics includes design partitioning hierarchy decomposition safe coding styles back annotation wrapper modules concurrency race conditions assertion based verification clock synchronization and design for test A concluding presentation of special topics includes System Verilog and Verilog AMS [ICT Systems and Sustainability](#) Milan Tuba,Shyam Akashe,Amit Joshi,2023-10-31 This book proposes new technologies and discusses future solutions for ICT design infrastructures as reflected in high quality

papers presented at the 8th International Conference on ICT for Sustainable Development ICT4SD 2023 held in Goa India on 3 4 August 2023 The book covers the topics such as big data and data mining data fusion IoT programming toolkits and frameworks green communication systems and network use of ICT in smart cities sensor networks and embedded system network and information security wireless and optical networks security trust and privacy routing and control protocols cognitive radio and networks and natural language processing Bringing together experts from different countries the book explores a range of central issues from an international perspective *Transforming Tomorrow: Innovative Solutions and Global Trends in Electrical and Electronics Engineering* Namit Gupta, Anjali Gupta, Naresh Purohit, Shiraz Husain, 2025-06-03

The International Conference on Transforming Tomorrow Innovative Solutions and Global Trends in Electrical and Electronics Engineering Pragya 2025 is scheduled to be held on May 5 6 2025 at Shri Vaishnav Vidyapeeth Vishwavidyalaya Indore Madhya Pradesh India This prestigious event aims to provide a dynamic platform for researchers academicians industry professionals and students to exchange knowledge showcase cutting edge innovations and discuss global trends shaping the future of Electrical and Electronics Engineering Pragya 2025 will feature sessions and presentations on key emerging areas including Robotics Renewable Energy Smart Grids Mechatronics 5G Communications Artificial Intelligence and the Internet of Things IoT The conference is designed to foster meaningful dialogue cross disciplinary collaboration and engagement with leading experts from academia and industry In line with its theme of Transforming Tomorrow the conference emphasizes clarity innovation and sustainable development It will serve as a catalyst for forward looking discussions and solutions that address modern engineering challenges and contribute to building a smarter greener and more connected world With a commitment to being Concise Clear and Cohesive Pragya 2025 is set to become a significant academic and professional milestone in advancing technological progress and inspiring future innovation across the Electrical and Electronics Engineering spectrum

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 lungs b blood c rectum 2 the excretory system consists of a rectum lungs skin and kidneys b rectum liver and kidneys c lungs  
 liver skin and kidneys 3 the wastes excreted from the lungs are a carbon dioxide and  
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 stimuli is sent and food is

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