

CS-200: Verilog Coding Style Guide

Learning Goal: Verilog Style.

Requirements: Verible.

1 Introduction

This document will teach you some guidelines for a readable and well-constituted Verilog.

We will use [Verible](#) as the linting tool for the labs. The tool does not cover all of the rules in this document; however, it comes in handy in detecting many problems that might exist in your Verilog code. We will run Verible on each submission and will **deduct half of the lab grade** if the code does not pass the linting with zero errors. We provide a `flags.txt` file alongside this document that shall be used as a configuration input to the Verible linter. The content of the `flags.txt` file can be found below with the command needed to run the linter on a Verilog file.

```
-always-comb
+port-name-suffix
signal-name-style="style_regex:[a-z_0-9]+'"
-explicit-parameter-storage-type
+parameter-name-style="localparam_style:ALL_CAPS;parameter_style:ALL_CAPS"
```

```
verible-verilog-lint {file} --rules_config flags.txt
```

2 General Guidelines

- **always@ (*)** is used to describe a block with combinational logic. The `*` symbol is used in the sensitivity list to trigger the block whenever any of the inputs are changed; therefore, the outputs reflect the inputs change.
- **always@ (posedge clk)** is used to describe a block with sequential logic i.e., has flip-flops. The two keywords **posedge** and **negedge** determine whether the active clock edge of the flip-flops is the rising or the falling clock edge respectively.
- Use blocking (`=`) assignments in **combinational** always blocks.
- Use nonblocking (`<=`) assignments in **edge-sensitive sequential** always blocks. Blocking assignments (`=`) are not allowed.
- Avoid latches in your sequential designs and use only D flip-flops. Latches might sneak into your combinational blocks; to avoid this, it is a good practice to start your combinational always block

Verilog Style Guide

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Verilog Style Guide:

SystemVerilog For Design Stuart Sutherland, Simon Davidmann, Peter Flake, 2013-12-01 SystemVerilog is a rich set of extensions to the IEEE 1364 2001 Verilog Hardware Description Language Verilog HDL These extensions address two major aspects of HDL based design First modeling very large designs with concise accurate and intuitive code Second writing high level test programs to efficiently and effectively verify these large designs This book SystemVerilog for Design addresses the first aspect of the SystemVerilog extensions to Verilog Important modeling features are presented such as two state data types enumerated types user defined types structures unions and interfaces Emphasis is placed on the proper usage of these enhancements for simulation and synthesis A companion to this book SystemVerilog for Verification covers the second aspect of SystemVerilog

SystemVerilog for Verification Chris Spear, 2008-04-22 SystemVerilog for Verification Second Edition provides practical information for hardware and software engineers using the SystemVerilog language to verify electronic designs The author explains methodology concepts for constructing testbenches that are modular and reusable The book includes extensive coverage of the SystemVerilog 3.1a constructs such as classes program blocks randomization assertions and functional coverage It also reviews SystemVerilog 3.0 topics such as interfaces and data types This second edition contains a new chapter that covers programs and interfaces as well as chapters with updated information on directed testbench and OOP layered and random testbench for an ATM switch This edition also includes a new chapter that covers Interfacing to C and many new and improved examples and explanations For hardware engineers the book has several chapters with detailed explanations of Object Oriented Programming based on years of teaching OOP to hundreds of students For software engineers there is a wealth of information on testbenches multithreaded code and interfacing to hardware designs The reader only needs to know the Verilog 1995 standard The complete book that covers verification concepts and use of system verilog in Verification taking your from an easy start to advanced concepts with ease Paul D Franzon Alumni Distinguished Professor of ECE North Carolina State University

Digital Design William James Dally, R. Curtis Harting, 2012-09-17 This book provides students with a system level perspective and the tools they need to understand analyze and design complete digital systems using Verilog It goes beyond the design of simple combinational and sequential modules to show how such modules are used to build complete systems reflecting digital design in the real world

Computer Hardware Description Languages and Their Applications David Agnew, Luc J. M. Claesen, Raul Camposano, 1993 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal

reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification **Not Just Java** Peter Van der Linden,1999 PLEASE PROVIDE *Reuse Techniques for VLSI Design* Ralf Seepold,Arno Kunzmann,2012-12-06

Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design *Digital System Design with SystemVerilog* Mark Zwolinski,2009-10-23 The Definitive Up to Date Guide to Digital Design with SystemVerilog Concepts Techniques and Code To design state of the art digital hardware engineers first specify functionality in a high level Hardware Description Language HDL and today s most powerful useful HDL is SystemVerilog now an IEEE standard Digital System Design with SystemVerilog is the first comprehensive introduction to both SystemVerilog and the contemporary digital hardware design techniques used with it Building on the proven approach of his bestselling Digital System Design with VHDL Mark Zwolinski covers everything engineers need to know to automate the entire design process with SystemVerilog from modeling through functional simulation synthesis timing simulation and verification Zwolinski teaches through about a hundred and fifty practical examples each with carefully detailed syntax and enough in depth information to enable rapid hardware design and verification All examples are available for download from the book s companion Web site zwolinski org Coverage includes Using electronic design automation tools with programmable logic and ASIC technologies Essential principles of Boolean algebra and combinational logic design with discussions of timing and hazards Core modeling techniques combinational building blocks buffers decoders encoders multiplexers adders and parity checkers Sequential building blocks latches flip

flops registers counters memory and sequential multipliers Designing finite state machines from ASM chart to D flip flops next state and output logic Modeling interfaces and packages with SystemVerilog Designing testbenches architecture constrained random test generation and assertion based verification Describing RTL and FPGA synthesis models Understanding and implementing Design for Test Exploring anomalous behavior in asynchronous sequential circuits Performing Verilog AMS and mixed signal modeling Whatever your experience with digital design older versions of Verilog or VHDL this book will help you discover SystemVerilog s full power and use it to the fullest **A Practical Guide for Simulation and FPGA Implementation of Digital Design** Bekkay Hajji, Adel Mellit, Loubna Bouselham, 2022-03-21 This book introduces the FPGA technology used in the laboratory sessions and provides a step by step guide for designing and simulation of digital circuits It utilizes the VHDL language which is one of the most common language used to describe the design of digital systems The Quartus II Xilinx ISE 14.7 and ModelSim software are used to process the VHDL code and make simulations and then the Altera and Xilinx FPGA platforms are employed to implement the simulated digital designs The book is composed of four parts The first part of this book has two chapters and covers various aspects FPGA architectures ASIC vs FPGA comparison FPGA design flow and basic VHDL concepts necessary to describe the design of digital systems The second part of the book includes three chapters that deal with the design of digital circuits such as combinational logic circuits sequential logic circuits and finite state machines The third part of the book is reserved for laboratory projects carried out on the FPGA platform It is a largely hands on lab class for design digital circuits and implementing their designs on the Altera FPGA platform Finally the fourth part of this work is devoted to recent applications carried out on FPGAs in particular advanced techniques in renewable energy systems The book is primarily intended for students scholars and industrial practitioners interested in the design of modern digital systems **Digital Design Using VHDL** William J. Dally, R. Curtis Harting, Tor M. Aamodt, 2016 Provides students with a system level perspective and the tools they need to understand analyze and design complete digital systems using VHDL It goes beyond the design of simple combinational and sequential modules to show how such modules are used to build complete systems reflecting digital design in the real world **FPGA/CPLD** [book] [author], 2005 Xilinx Altera FPGA CPLD FPGA CPLD MAX plus II Quartus ISE Verilog VHDL LED LCD ISA PCI FPGA CPLD "Looks Good to Me" Adrienne Braganza, 2025-01-07 Deliver code reviews that consistently build up your team and improve your applications Looks Good to Me offers a unique approach to delivering meaningful code reviews that goes beyond superficial checklists and tense critical conversations Instead you ll learn how to improve both your applications and your team dynamics Looks Good to Me teaches you how to Understand a code review s benefits proactively prevent loopholes and bottlenecks Co create an objective code review system Clarify responsibilities author reviewer team lead manager and the team itself Establish manageable guidelines and protocols Align with your team and explicitly document the policies they will follow Automate code quality with linting formatting static analysis and automated testing Compose effective comments

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Languages for System Specification
 Christoph Grimm,1996-12-15 Contributions on UML address the application of UML in the specification of embedded HW SW systems C Based System Design embraces the modeling of operating systems modeling with different models of computation generation of test patterns and experiences from case studies with SystemC Analog and Mixed Signal Systems covers rules for solving general modeling problems in VHDL AMS modeling of multi nature systems synthesis and modeling of Mixed Signal Systems with SystemC Languages for formal methods are addressed by contributions on formal specification and refinement of hybrid embedded and real time stems Together with articles on new languages such as SystemVerilog and Software Engineering in Automotive Systems the contributions selected for this book embrace all aspects of languages and models for specification design modeling and verification of systems Therefore the book gives an excellent overview of the actual state of the art and the latest research results

Using PSL/Sugar for Formal and Dynamic Verification Ben Cohen,Srinivasan Venkataramanan,Ajeetha Kumari,2004

Writing Testbenches using SystemVerilog Janick Bergeron,2007-02-02 Verification is too often approached in an ad hoc fashion Visually inspecting simulation results is no

longer feasible and the directed test case methodology is reaching its limit Moore's Law demands a productivity revolution in functional verification methodology Writing Testbenches Using SystemVerilog offers a clear blueprint of a verification process that aims for first time success using the SystemVerilog language From simulators to source management tools from specification to functional coverage from I s and O s to high level abstractions from interfaces to bus functional models from transactions to self checking testbenches from directed testcases to constrained random generators from behavioral models to regression suites this book covers it all Writing Testbenches Using SystemVerilog presents many of the functional verification features that were added to the Verilog language as part of SystemVerilog Interfaces virtual modports classes program blocks clocking blocks and others SystemVerilog features are introduced within a coherent verification methodology and usage model Writing Testbenches Using SystemVerilog introduces the reader to all elements of a modern scalable verification methodology It is an introduction and prelude to the verification methodology detailed in the Verification Methodology Manual for SystemVerilog It is a SystemVerilog version of the author's bestselling book Writing Testbenches Functional Verification of HDL Models *Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL* Michael D. Ciletti,1999 Verilog aims to introduce new users to the language of Verilog with instruction on how to write hardware descriptions in Verilog in a style that can be synthesized by readily available synthesis tools Offers clear exposition of the Verilog hardware description language This book is written in a style that allows the user who has no previous background with hardware description languages HDLs to become skillful with the language Features treatment of synthesis friendly descriptive styles An excellent book for self study reference seminars and workshops on the subject *SystemVerilog Assertions Handbook* Ben Cohen,Srinivasan Venkataramanan,Ajeetha Kumari,2005 **A Practical Approach to VLSI System on Chip (SoC) Design** Veena S. Chakravarthi,2022-12-13 Now in a thoroughly revised second edition this practical practitioner guide provides a comprehensive overview of the SoC design process It explains end to end system on chip SoC design processes and includes updated coverage of design methodology the design environment EDA tool flow design decisions choice of design intellectual property IP cores sign off procedures and design infrastructure requirements The second edition provides new information on SOC trends and updated design cases Coverage also includes critical advanced guidance on the latest UPF based low power design flow challenges of deep submicron technologies and 3D design fundamentals which will prepare the readers for the challenges of working at the nanotechnology scale A Practical Approach to VLSI System on Chip SoC Design A Comprehensive Guide Second Edition provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools It will be a valuable professional reference for those working on VLSI design and verification portfolios in complex SoC designs **Digital Design (VHDL)** Peter J. Ashenden,2007-10-24 Digital Design An Embedded Systems Approach Using VHDL provides a foundation in digital design for students in computer engineering electrical engineering and computer science courses It takes an up to date and modern

approach of presenting digital logic design as an activity in a larger systems design context Rather than focus on aspects of digital design that have little relevance in a realistic design context this book concentrates on modern and evolving knowledge and design skills Hardware description language HDL based design and verification is emphasized VHDL examples are used extensively throughout By treating digital logic as part of embedded systems design this book provides an understanding of the hardware needed in the analysis and design of systems comprising both hardware and software components Includes a Web site with links to vendor tools labs and tutorials Presents digital logic design as an activity in a larger systems design context Features extensive use of VHDL examples to demonstrate HDL hardware description language usage at the abstract behavioural level and register transfer level as well as for low level verification and verification environments Includes worked examples throughout to enhance the reader s understanding and retention of the material Companion Web site includes links to tools for FPGA design from Synplicity Mentor Graphics and Xilinx VHDL source code for all the examples in the book lecture slides laboratory projects and solutions to exercises *High-level Synthesis* Michael Fingeroff,2010 Are you an RTL or system designer that is currently using moving or planning to move to an HLS design environment Finally a comprehensive guide for designing hardware using C is here Michael Fingeroff s High Level Synthesis Blue Book presents the most effective C synthesis coding style for achieving high quality RTL Master a totally new design methodology for coding increasingly complex designs This book provides a step by step approach to using C as a hardware design language including an introduction to the basics of HLS using concepts familiar to RTL designers Each chapter provides easy to understand C examples along with hardware and timing diagrams where appropriate The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub system design Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples These examples illustrate the fundamental principles behind C hardware design which will translate to much larger designs Although this book focuses primarily on C and C to present the basics of C synthesis all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design On completion of this book readers should be well on their way to becoming experts in high level synthesis *SystemVerilog* [SystemVerilog](#) [FPGA](#) [ASIC](#) [SystemVerilog](#) [Verilog](#) [HDL](#) [Verilog](#) [HDL](#) [VHDL](#) [SystemVerilog](#) [FPGA](#) [SystemVerilog](#) [RISC](#) [V](#) [Verilog](#) [HDL](#) [maker](#) [1](#) [FPGA](#) [ASIC](#) [2](#) [FPGA](#) [3](#) [4](#) [SystemVerliog](#) [5](#) [SystemVerilog](#) [FPGA](#) [6](#) [SystemVerilog](#) [ASIC](#) [7](#) [SystemVerilog](#) [Verilog](#) [HDL](#)

Decoding **Verilog Style Guide**: Revealing the Captivating Potential of Verbal Expression

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
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