## VLSI Physical Design

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#### Saturday, 20 February 2016

### STA Interview Questions Part 1 White is stack? What is SDC constraint the contains? Delay of a cell depends on which factors 7 With Setup and Hold equations? Where do you get the WUM's? Do you create WUM's? How do you specify? In which case inserting a buffer will solve the setup timing? What is cross talk? How it affects timing. How can you avoid cross talk? what is shielding ? how doe it prevents cross talk ? How spacing helps in reducing crosstalk noise? How buffer can be used in victim to avoid crosstalk? What are the problems faced related to timing? How did you resolve the setup and hold problem? How does delays varies with different PVT conditions? please explain with the help of graph. What is cell delay and net delay? What are different delay models available and what are the difference between them? What is cloning and buffering? What is the derate value that can be used? What are the corners you check for timing sign-off? Is there any changes in the derate value for each Where do you mean by the de-rating value? What are the factors that decide the de-rating values? What factors decides the setup time of tip-top? What is meta-stability? in a system with insufficient hold time, will slowing down the clock frequency help? Posted by Akshay at 22:43

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