

FACULTY OF ENGINEERING**B.E. 4/4 (ECE) I - Semester (Main) Examination, December/January 2014-15****Subject : VLSI Design****Time : 3 Hours****Max. Marks: 75**

Note: Answer all questions of Part - A and answer any five questions from Part-B.
PART – A (25 Marks)

- 1 What are the basic components of a verilog module? (2)
- 2 What is the difference between a gate instantiation and module instantiation? (2)
- 3 Distinguish between procedure and function declarations in verilog. (2)
- 4 Draw the synthesis process flowchart. (3)
- 5 Draw the basic pseudo nMOS inverter and give the relative merits and demerits of the same with respect to CMOS. (3)
- 6 State the significance of design rules. (2)
- 7 Draw the stick diagram of CMOS 2 input XOR gate. (3)
- 8 Write the expressions for Rise time, fall time and maximum signal frequency. (3)
- 9 Draw the schematic diagram of D-flip flop using Transmission gates. (2)
- 10 Draw the circuit diagram of six Transistor RAM Cell. (3)

PART – B (50 Marks)

- 11 (a) Differentiate blocking and non-blocking assignments with suitable examples. (4)
- (b) Write a verilog code and its test bench for a 4-bit comparator. (6)
- 12 Explain briefly about FSM module. Develop a verilog code for mealy model for 4 states. Assume present state, next state and output. (10)
- 13 (a) Explain the operation of n-channel Depletion mode MOSFET with neat diagrams and characteristic curves. (5)
- (b) Derive the expression for pull up to pull down ratio of an NMOS inverter driven by another nMOS inverter. (5)
- 14 (a) With suitable sketches explain the main steps that are followed in standard Si CMOS fabrication process. (6)
- (b) Draw the Transmission Gate based XOR and XNOR circuits. (4)
- 15 (a) Draw the stick diagrams and Layouts of Transmission gate and two input NAND gate. (6)
- (b) How to estimate Resistance and capacitance of a MOS Transistor? (4)
- 16 (a) Explain the operation of Manchester carry adder with neat diagrams. (5)
- (b) Draw the logic diagram of 8-bit NOR based ROM and explain its operation. (5)
- 17 Write short notes on the following:
 - (a) carry skip adder (5)
 - (b) Continuous assignment and delays in dataflow modeling (5)

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Yijin Wang



Vlsi Design Ece Previous Years Question Paper:

Basic VLSI Design Technology Cherry Bhargava, Gaurav Mani Khanal, 2022-09-01 The current cutting edge VLSI circuit design technologies provide end users with many applications increased processing power and improved cost effectiveness This trend is accelerating with significant implications on future VLSI and systems design VLSI design engineers are always in demand for front end and back end design applications The book aims to give future and current VLSI design engineers a robust understanding of the underlying principles of the subject It not only focuses on circuit design processes obeying VLSI rules but also on technological aspects of fabrication The Hardware Description Language HDL Verilog is explained along with its modelling style The book also covers CMOS design from the digital systems level to the circuit level The book clearly explains fundamental principles and is a guide to good design practices The book is intended as a reference book for senior undergraduate first year post graduate students researchers as well as academicians in VLSI design electronics electrical engineering and materials science The basics and applications of VLSI design from digital system design to IC fabrication and FPGA Prototyping are each covered in a comprehensive manner At the end of each unit is a section with technical questions including solutions which will serve as an excellent teaching aid to all readers Technical topics discussed in the book include Digital System Design Design flow for IC fabrication and FPGA based prototyping Verilog HDL IC Fabrication Technology CMOS VLSI Design Miscellaneous It covers basics of Electronics and Reconfigurable computing PLDs Latest technology etc

VLSI Design and Test Anirban Sengupta, Sudeb Dasgupta, Virendra Singh, Rohit Sharma, Santosh Kumar Vishvakarma, 2019-08-17 This book constitutes the refereed proceedings of the 23st International Symposium on VLSI Design and Test VDAT 2019 held in Indore India in July 2019 The 63 full papers were carefully reviewed and selected from 199 submissions The papers are organized in topical sections named analog and mixed signal design computing architecture and security hardware design and optimization low power VLSI and memory design device modelling and hardware implementation

Practical Problems in VLSI Physical Design Automation Sung Kyu Lim, 2008-07-31 Practical Problems in VLSI Physical Design Automation contains problems and solutions related to various well known algorithms used in VLSI physical design automation Dr Lim believes that the best way to learn new algorithms is to walk through a small example by hand This knowledge will greatly help understand analyze and improve some of the well known algorithms The author has designed and taught a graduate level course on physical CAD for VLSI at Georgia Tech Over the years he has written his homework with such a focus and has maintained typeset version of the solutions

Principles of VLSI and CMOS Integrated Circuits Jain Richa & Rai Amrita, 2016 For B E B Tech students of all Technical Universities

Microelectronics VLSI Design is an emerging subject in the field of electronics in recent years It is an introductory source to internal parts of electronics at minute level This book is covering CMOS Design from a digital system level to circuit level and providing a background in CMOS Processing Technology The book includes basic theoretical knowledge as well as good

engineering practice This book is recommended for B Tech M Tech and diploma students of all Indian Universities and also useful for competitive examinations

Model and Design of Improved Current Mode Logic Gates Kirti Gupta, Neeta Pandey, Maneesha Gupta, 2019-11-22 This book presents MOSFET based current mode logic CML topologies which increase the speed and lower the transistor count supply voltage and power consumption The improved topologies modify the conventional PDN load and the current source sections of the basic CML gates Electronic system implementation involves embedding digital and analog circuits on a single die shifting towards mixed mode circuit design The high resolution low power and low voltage analog circuits are combined with high frequency complex digital circuits and the conventional static CMOS logic generates large current spikes during the switching also referred to as digital switching noise which degrade the resolution of the sensitive analog circuits via supply line and substrate coupling This problem is exacerbated further with scaling down of CMOS technology due to higher integration levels and operating frequencies In the literature several methods are described to reduce the propagation of the digital switching noise However in high resolution applications these methods are not sufficient The conventional CMOS static logic is no longer an effective solution and therefore an alternative with reduced current spikes or that draws a constant supply current must be selected The current mode logic CML topology with its unique property of requiring constant supply current is a promising alternative to the conventional CMOS static logic

18th International Conference on VLSI Design International Conference on VLSI Design, 2005 **VLSI Design and Test** S. Rajaram, N.B. Balamurugan, D. Gracia Nirmala Rani, Virendra Singh, 2019-01-24 This book constitutes the refereed proceedings of the 22st International Symposium on VLSI Design and Test VDAT 2018 held in Madurai India in June 2018 The 39 full papers and 11 short papers presented together with 8 poster papers were carefully reviewed and selected from 231 submissions The papers are organized in topical sections named digital design analog and mixed signal design hardware security micro bio fluidics VLSI testing analog circuits and devices network on chip memory quantum computing and NoC sensors and interfaces

VLSI Design: Circuits, Systems and Applications Jie Li, A Ravi Sankar, P Augusta Sophy Beulet, 2018-01-02 This book gathers a collection of papers by international experts presented at the International Conference on NextGen Electronic Technologies ICNETS2 2017 which cover key developments in the field of electronics and communication engineering ICNETS2 encompassed six symposia covering all aspects of the electronics and communications domains including relevant nano micro materials and devices This book showcases the latest research in very large scale integration VLSI Design Circuits Systems and Applications making it a valuable resource for all researchers professionals and students working in the core areas of electronics and their applications especially in digital and analog VLSI circuits and systems

Proceedings American Society for Engineering Education. Conference, 1994 *Proceedings of ASP-DAC/VLSI Design 2002*, 2002 Papers from a January 2002 conference are organized into four sessions each on low power design synthesis testing layout and interconnects and technology as well as two sessions each on embedded systems verification and

VLSI architecture one session on analog design and one session on hot c **Progress in VLSI Design and Test** Hafizur Rahaman, Sanatan Chattopadhyay, Santanu Chattopadhyay, 2012-06-26 This book constitutes the refereed proceedings of the 16th International Symposium on VLSI Design and Test VDAT 2012 held in Shibpur India in July 2012 The 30 revised regular papers presented together with 10 short papers and 13 poster sessions were carefully selected from 135 submissions The papers are organized in topical sections on VLSI design design and modeling of digital circuits and systems testing and verification design for testability testing memories and regular logic arrays embedded systems hardware software co design and verification emerging technology nanoscale computing and nanotechnology **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Vassilis Paliouras, Johan Vounckx, Diederik Verkest, 2005-08-25 Welcome to the proceedings of PATMOS 2005 the 15th in a series of international workshops PATMOS2005 was organized by IMEC with technical co sponsorship from the IEEE Circuits and Systems Society Over the years PATMOS has evolved into an important European event where searchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications design methodologies and tools required for the development of upcoming generations of integrated circuits and systems The technical program of PATMOS 2005 contained state of the art technical contributions three invited talks a special session on hearing aid design and an embedded tutorial The technical program focused on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization in the nanometer era The Technical Program Committee with the assistance of additional expert reviewers selected the 74 papers to be presented at PATMOS The papers were divided into 11 technical sessions and 3 poster sessions As is always the case with the PATMOS workshops the review process was anonymous full papers were required and several reviews were carried out per paper Beyond the presentations of the papers the PATMOS technical program was enriched by a series of speeches offered by world class experts on important emerging research issues of industrial relevance Prof Jan Rabaey Berkeley USA gave a talk on Traveling the Wild Frontier of Ultra Low Power Design Dr Sung Bae Park S sung gave a presentation on DVL Deep Low Voltage Circuits and Devices Prof *Microelectronics, Electromagnetics and Telecommunications* Ganapati Panda, Suresh Chandra Satapathy, Birendra Biswal, Ramesh Bansal, 2018-11-02 The book discusses the latest developments and outlines future trends in the fields of microelectronics electromagnetics and telecommunication It contains original research works presented at the International Conference on Microelectronics Electromagnetics and Telecommunication ICMEET 2018 organised by GVP College of Engineering A Andhra Pradesh India The respective papers were written by scientists research scholars and practitioners from leading universities engineering colleges and R D institutes from all over the world and share the latest breakthroughs in and promising solutions to the most important issues facing today's society High Performance Computing for Computational Science - VECPAR 2012 Michel Dayde, Osni Marques, Kengo Nakajima, 2013-05-24 This book constitutes the

thoroughly refereed post conference proceedings of the 10th International Conference on High Performance Computing for Computational Science VECPAR 2012 held in Kope Japan in July 2012 The 28 papers presented together with 7 invited talks were carefully selected during two rounds of reviewing and revision The papers are organized in topical sections on CPU computing applications finite element method from various viewpoints cloud and visualization performance method and tools for advanced scientific computing algorithms and data analysis parallel iterative solvers on multicore architectures RF Circuits for 5G Applications Sangeeta Singh,Rajeev Kumar Arya,B. C. Sahana,Ajay Kumar Vyas,2023-03-10 RF CIRCUITS FOR 5G APPLICATIONS This book addresses FinFET based analog IC designing for fifth generation 5G communication networks and highlights the latest advances problems and challenges while presenting the latest research results in the field of mmwave integrated circuits designing The wireless communication sector is experiencing exponential expansion particularly in the areas of mobile data and the 5G mobile network creating fresh market possibilities for designing the integrated circuits ICs needed in the industry Drawing from scientific literature and practical realization this book explores FinFET based analog IC designing for 5G communication networks and considers the latest breakthroughs and obstacles It also presents the recent research trends and future roadmaps for the 5G communication circuits RF Circuits for 5G Applications includes design guidelines to be considered when designing these circuits and detrimental scaling effects of the same In addition to enhance the usability of this book the editors have included real time problems in RFIC designing and case studies from experimental results as well as clearly demarcated design guidelines for the 5G communication ICs designing Audience The primary target audience includes researchers postgraduate students and industry professionals pursuing specializations in RF engineering electronics engineering electrical engineering information and communication technology **Transactions on High-Performance Embedded Architectures and Compilers IV** Per Stenström,2011-11-22 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 4th issue contains 21 papers carefully reviewed and selected out of numerous submissions and is divided in four sections The first section contains five regular papers The second section consists of the top four papers from the 4th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2009 held in Paphos Cyprus in January 2009 The third section contains a set of six papers providing a snap shot from the Workshop on Software and Hardware Challenges of Manycore Platforms SHCMP 2008 held in Beijing China in June 2008 The fourth section consists of six papers from the 8th IEEE International Symposium on Systems Architectures Modeling and

Simulation SAMOS VIII 2008 held in Samos Greece in July 2008 Emerging VLSI Devices, Circuits and Architectures Anu Gupta, Jai Gopal Pandey, Nitin Chaturvedi, Devesh Dwivedi, 2024-10-18 This book constitutes the proceedings of the 27th International Symposium on VLSI Design and Test VDAT 2023 The 32 regular papers and 16 short papers presented in this book are carefully reviewed and selected from 220 submissions They are organized in topical sections as follows Low Power Integrated Circuits and Devices FPGA Based Design and Embedded Systems Memory Computing and Processor Design CAD for VLSI Emerging Integrated Circuits and Systems VLSI Testing and Security and System Level Design **Tutorials on Emerging Methodologies and Applications in Operations Research** Harvey J. Greenberg, 2006-06-16 This volume reflects the theme of the INFORMS 2004 Meeting in Denver Back to OR Roots Emerging as a quantitative approach to problem solving in World War II our founders were physicists mathematicians and engineers who quickly found peace time uses It is fair to say that Operations Research OR was born in the same incubator as computer science and it has spawned many new disciplines such as systems engineering health care management and transportation science Although people from many disciplines routinely use OR methods many scientific researchers engineers and others do not understand basic OR tools and how they can help them Disciplines ranging from finance to bioengineering are the beneficiaries of what we do we take an interdisciplinary approach to problem solving Our strengths are modeling analysis and algorithm design We provide a quantitative foundation for a broad spectrum of problems from economics to medicine from environmental control to sports from e commerce to computational ometry We are both producers and consumers because the mainstream of OR is in the interfaces As part of this effort to recognize and extend OR roots in future probl solving we organized a set of tutorials designed for people who heard of the topic and want to decide whether to learn it The 90 minutes was spent addre ing the questions What is this about in a nutshell Why is it important Where can I learn more In total we had 14 tutorials and eight of them are published here Computer, Communication and Electrical Technology Debatosh Guha, Badal Chakraborty, Himadri Sekhar Dutta, 2017-03-16 The First International Conference on Advancement of Computer Communication and Electrical Technology focuses on key technologies and recent progress in computer vision information technology applications VLSI signal processing power electronics drives and application of sensors transducers etc Topics in this conference include Computer Science This conference encompassed relevant topics in computer science such as computer vision intelligent system networking theory and application of information technology Communication Engineering To enhance the theory technology of communication engineering ACCET 2016 highlighted the state of the art research work in the field of VLSI optical communication and signal processing of various data formatting Research work in the field of microwave engineering cognitive radio and networks are also included Electrical Technology The state of the art research topic in the field of electrical instrumentation engineering is included in this conference such as power system stability protection non conventional energy resources electrical drives and biomedical engineering Research work in the area of

optimization and application in control measurement instrumentation are included as well Power-Aware Computer Systems B. Falsafi, T.N. Vijaykumar, 2003-05-15 The phenomenal increases in computer system performance in recent years have been accompanied by a commensurate increase in power and energy dissipation The latter has directly resulted in demand for expensive packaging and cooling technology an increase in product cost and a decrease in product reliability in all segments of the computing market Moreover the higher power energy dissipation has significantly reduced battery life in portable systems While system designers have traditionally relied on circuit level techniques to reduce power energy there is a growing need to address power energy dissipation at all levels of the computer system We are pleased to welcome you to the proceedings of the Power Aware Computer Systems PACS 2000 workshop PACS 2000 was the first workshop in its series and its aim was to bring together experts from academia and industry to address power energy awareness at all levels of computer systems In these proceedings we bring you several excellent research contributions spanning a wide spectrum of areas in power aware systems from application all the way to compilers and microarchitecture and to power performance estimating models and tools We have grouped the contributions into the following specific categories 1 power aware microarchitectural circuit techniques 2 application compiler power optimizations 3 exploiting opportunity for power optimization in instruction scheduling and cache memories and 4 power performance models and tools

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