First Semester M.Tech. Degree Examination, June/July 2015
Digital VLSI Design

Time: 3 hrs.　　　　　　　　　　　　　　　　　　　　　Max. Marks: 100

Note: *Answer any FIVE full questions.*

1 a. Discuss gradual channel approximation concept in MOSFET and derive the current expression for MOSFET operating in saturation region　(10 Marks)

  b. Discuss the second order effects of MOSFET and arrive at current expression for MOSFET in saturation region considering channel length modulation.　(06 Marks)

  c. Discuss how constant voltage scaling affects the current and power characteristics of MOSFET.　(04 Marks)

2 a. Discuss the voltage transfer characteristics of CMOS inverter mentioning the regions of operation and input and output voltages.　(06 Marks)

  b. Calculate V_{TH} for a CMOS inverter when $k_n = k_p$, $k_n = 2 k_p$ and $k_n = k_p/2$ with $V_{To n} = 0.6$ V, $V_{To p} = -0.7$ V and $V_{DD} = 3.3$ V. From the calculations, discuss how variations in k_n and k_p affects V_{TH}?　(08 Marks)

  c. With the neat schematic, mention the parasitic capacitances in the CMOS inverter?　(06 Marks)

3 a. Explain the concept of voltage bootstrapping.　(05 Marks)

  b. Discuss the charge sharing problem in CMOS circuits. Explain the various techniques used in domino CMOS logic for solving charge sharing problem.　(10 Marks)

  c. Design negative edge triggered D – Flipflop using true single phase clock (TSPC) dynamic CMOS logic.　(05 Marks)

4 a. Design 4 × 8 NOR based ROM array that can store the following data given in table 4(a). Note : R_1, R_2, R_3 R_4 → Address and C_1, C_2, C_3 C_4 C_5, C_6, C_7, C_8 → Memory Locations.　(06 Marks)

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
1	0	0	0	0	1	0	1	0	1	0	0
0	1	0	0	1	1	1	0	0	1	0	0
0	0	1	0	1	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	0	1	1	1

  b. Draw a neat schematic of 6 T SRAM cell and discuss write 'O' and read 'O' operation?　(10 Marks)

  c. Explain the working principle of 3T DRAM cell.　(04 Marks)

5 a. Discuss CMOS switching power dissipation and derive the expression for average switching power dissipation.　(06 Marks)

  b. CMOS circuit consisting of 20 nodes with power consuming voltage transition (α_T) per clock cycle consumes a power of 10 μW for a give $C_{load} = 0.1$ pF and $V_{DD} = 1.8$ V. Find the maximum operating frequency of the CMOS circuit if the mode transitions is increased from 20 to 30. What is the change in switching power dissipation?　(08 Marks)

  c. Discuss briefly variable threshold CMOS and multi threshold CMOS circuits.　(06 Marks)

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Principles of VLSI and CMOS Integrated Circuits Jain Richa & Rai Amrita,2016 For B E B Tech students of all Technical Universities Microelectronics VLSI Design is an emerging subject in the field of electronics in recent years It is an introductory source to internal parts of electronics at minute level This book is covering CMOS Design from a digital system level to circuit level and providing a background in CMOS Processing Technology The book includes basic theortical knowledge as well as good engineering practice This book is recommended for B Tech M Tech and diploma students of all Indian Universities and also useful for competitive examinations   Basic Electronics Rakesh Kumar Garg,Ashish Dixit,Pavan Yadav,2008   **VLSI Design and Test** Manoj Singh Gaur,Mark Zwolinski,Vijay Laxmi,D. Boolchandani,Virendra Sing,Adit Singh,2013-12-13 This book constitutes the refereed proceedings of the 17th International Symposium on VLSI Design and Test VDAT 2013 held in Jaipur India in July 2013 The 44 papers presented were carefully reviewed and selected from 162 submissions The papers discuss the frontiers of design and test of VLSI components circuits and systems They are organized in topical sections on VLSI design testing and verification embedded systems emerging technology   *Integrated Circuits MCQ (Multiple Choice Questions)* Arshad Iqbal, The Integrated Circuits Multiple Choice Questions MCQ Quiz with Answers PDF Integrated Circuits MCQ PDF Download Quiz Questions Chapter 1 2 Practice Tests with Answer Key Electronics Questions Bank MCQs Notes includes revision guide for problem solving with hundreds of solved MCQs Integrated Circuits MCQ with Answers PDF book covers basic concepts analytical and practical assessment tests Integrated Circuits MCQ PDF book helps to practice test questions from exam prep notes The Integrated Circuits MCQs with Answers PDF eBook includes revision guide with verbal quantitative and analytical past papers solved MCQs Integrated Circuits Multiple Choice Questions and Answers MCQs PDF Free download chapter 1 a book covers solved quiz questions and answers on chapters Introduction to digital integrated circuits MOSFETs tests for college and university revision guide Integrated Circuits Quiz Questions and Answers PDF free download eBook s sample covers beginner s solved questions textbook s study notes to practice online tests The book Integrated Circuits MCQs Chapter 1 2 PDF includes high school question papers to review practice tests for exams Integrated Circuits Multiple Choice Questions MCQ with Answers PDF digital edition eBook a study guide with textbook chapters tests for NEET Jobs Entry Level competitive exam Integrated Circuits Mock Tests Chapter 1 2 eBook covers problem solving exam tests from electronics engineering textbook and practical eBook chapter wise as Chapter 1 Introduction to Digital Integrated Circuits MCQ Chapter 2 MOSFETs MCQ The Introduction to Digital Integrated Circuits MCQ PDF e Book Chapter 1 practice test to solve MCQ questions on BSIM family challenges in digital design CMOS transistors cost of integrated circuits design abstraction levels digital and analog signal gate level modeling introduction to analog and digital circuits Moore s law MOSFET as switch multigate devices Pentium 4 power dissipation sources scaling SOI technology spice supercomputers switching activity factor and VLSI design flow The MOSFETs MCQ PDF e Book

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good grades using thoroughly Researched Content by experts **Digital VLSI Design with Verilog** John Williams,2008-06-06 Verilog and its usage has come a long way since its original invention in the mid 80s by Phil Moorby At the time the average design size was around ten thousand gates and simulation to validate the design was its primary usage But between then and now designs have increased dramatically in size and automatic logic synthesis from RTL has become the standard design ow for most design Indeed the language has evolved and been re standardized too Overtheyears manybookshavebeenwrittenaboutVerilog Myown coauthored with Phil Moorby had the goal of de ning the language and its usage providing amples along the way It has been updated with ve new editions as the language and its usage evolved However this new book takes a very different and unique view that of the designer John Michael Williams has a long history of working and teaching in the eld of IC and ASIC design He brings an indepth presentation of Verilog and how to use it with logic synthesis tools no other Verilog book has dealt with this topic as deeply as he has If you need to learn Verilog and get up to speed quickly to use it for synthesis this book is for you It is sectioned around a set of lessons including presentation and explanation of new concepts and approaches to design along with lab sessions **VLSI Design Methodologies for Digital Signal Processing Architectures** Magdy A. Bayoumi,2012-12-06 Designing VLSI systems represents a challenging task It is a transfonnation among different specifications corresponding to different levels of design abstraction behavioral stntctural and physical The behavioral level describes the functionality of the design It consists of two components static and dynamic The static component describes operations whereas the dynamic component describes sequencing and timing The structural level contains infonnation about components control and connectivity The physical level describes the constraints that should be imposed on the floor plan the placement of components and the geometry of the design Constraints of area speed and power are also applied at this level To implement such multilevel transfonnation a design methodology should be devised taking into consideration the constraints limitations and properties of each level The mapping process between any of these domains is non isomorphic A single behavioral component may be transfonned into more than one structural component Design methodologies are the most recent evolution in the design automation era which started off with the introduction and subsequent usage of module generation especially for regular structures such as PLA s and memories A design methodology should offer an integrated design system rather than a set of separate unrelated routines and tools A general outline of a desired integrated design system is as follows Decide on a certain unified framework for all design levels Derive a design method based on this framework Create a design environment to implement this design method *Study of Engineering and Career* J Vinay Kumar,2018-04-20 There are many ways to apply knowledge to achieve a successful career Different people have used different ideologies get to the top What are the characteristics that will help you achieve success This book caters not only to students stepping into the engineering fields or the corporate world for the first time but also to those who are stuck in the wrong profession The book highlights the importance of knowing your field of education the

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