

First Semester M.Tech. Degree Examination, Dec.2014/Jan.2015
Digital VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

1.
 - a. Derive the equations for I_{ds} for all 3-regions starting from fundamentals. (10 Marks)
 - b. How do you change the above equation to reflect the effect of channel length modulation? (04 Marks)
 - c. Calculate I_{ds} for nMOS enhancement transistor for following conditions:
 i) $V_{gs} = 0.7V$ ii) $V_{gs} = 2V$, $\lambda = 0$ iii) $V_{gs} = 2V$, $\lambda = 0.15/V$. Given:
 $\mu_n = 600 \text{ cm}^2/V\cdot\text{s}$, $C_{ox} = 7 \times 10^{-6} \text{ F/cm}^2$, $V_{th} = 1V$, $V_{DS} = 5V$, $W = 20\mu\text{m}$, $L = 20\mu\text{m}$. (06 Marks)
2.
 - a. Derive expressions for V_{DD} , V_{IL} and V_{OH} for CMOS inverter. (10 Marks)
 - b. Derive the relation between $(W/L)_n$ and $(W/L)_p$ for symmetric CMOS inverter. Also discuss the effect of K_n variations on VTC. (08 Marks)
 - c. Discuss the enhancement load nMOS inverter. (04 Marks)
3.
 - a. Define propagation delays and derive the expression for t_{PHL} and t_{PLH} for CMOS inverter using differential equation method. (10 Marks)
 - b. Explain 3-stage CMOS ring oscillator. (06 Marks)
 - c. Calculate the total resistance and total capacitance for uniform polysilicon line with length of $1000\mu\text{m}$ and a width of $4\mu\text{m}$. Given: sheet resistance $30\Omega/\text{square}$, unit area capacitance $0.066\text{fF}/\mu\text{m}^2$, unit length capacitance $0.046 \text{ fF}/\mu\text{m}$. (04 Marks)
4.
 - a. What is dynamic CMOS logic? Explain with aid of an example. (06 Marks)
 - b. Illustrate the cascading problem in a dynamic CMOS logic. How is it overcome? (06 Marks)
 - c. Discuss the dynamic voltage bootstrapping circuit with necessary mathematical equations. (08 Marks)
5.
 - a. Discuss the 3-transistor DRAM cell with read and write operations. (10 Marks)
 - b. Explain memory structure SRAM with read and write circuitry with aid of read and write timing diagram. (10 Marks)
6.
 - a. What is short circuit power dissipation? On what parameters does it depend? (10 Marks)
 - b. Describe the types of threshold CMOS circuits used to minimize dynamic power consumption in CMOS digital ICs. (10 Marks)
7.
 - a. Differentiate between CMOS and BiCMOS. (05 Marks)
 - b. Explain the static characteristics of resistive load BJT inverter. (07 Marks)
 - c. Draw the BiCMOS circuits for the following with nMOS transistor for removing the base charge of bipolar transistor. i) $y = \overline{A}$ ii) $y = \overline{A + B}$ iii) $y = \overline{A \cdot B}$. (08 Marks)
8.
 - a. What is the latch-up problem that arises in bulk CMOS technology? (08 Marks)
 - b. Give any 5 guide lines for avoiding latch-up. (05 Marks)
 - c. With aid of diagram explain the performance modeling procedure. (07 Marks)

Vlsi Desine Questionpaper

**Rakesh Kumar Garg,Ashish
Dixit,Pavan Yadav**



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Principles of VLSI and CMOS Integrated Circuits Jain Richa & Rai Amrita, 2016 For B E B Tech students of all Technical Universities Microelectronics VLSI Design is an emerging subject in the field of electronics in recent years It is an introductory source to internal parts of electronics at minute level This book is covering CMOS Design from a digital system level to circuit level and providing a background in CMOS Processing Technology The book includes basic theortical knowledge as well as good engineering practice This book is recommended for B Tech M Tech and diploma students of all Indian Universities and also useful for competitive examinations **Basic Electronics** Rakesh Kumar Garg, Ashish Dixit, Pavan Yadav, 2008 **VLSI Design and Test** Manoj Singh Gaur, Mark Zwolinski, Vijay Laxmi, D. Boolchandani, Virendra Sing, Adit Singh, 2013-12-13 This book constitutes the refereed proceedings of the 17th International Symposium on VLSI Design and Test VDAT 2013 held in Jaipur India in July 2013 The 44 papers presented were carefully reviewed and selected from 162 submissions The papers discuss the frontiers of design and test of VLSI components circuits and systems They are organized in topical sections on VLSI design testing and verification embedded systems emerging technology **VLSI-SoC: System-on-Chip in the Nanoscale Era - Design, Verification and Reliability** Thomas Hollstein, Jaan Raik, Sergei Kostin, Anton Tšertov, Ian O'Connor, Ricardo Reis, 2017-08-31 This book contains extended and revised versions of the best papers presented at the 24th IFIP WG 10.5 IEEE International Conference on Very Large Scale Integration VLSI SoC 2016 held in Tallinn Estonia in September 2016 The 11 papers included in the book were carefully reviewed and selected from the 36 full papers presented at the conference The papers cover a wide range of topics in VLSI technology and advanced research They address the latest scientific and industrial results and developments as well as future trends in the field of System on Chip SoC Design *VLSI Design and Test* Brajesh Kumar Kaushik, Sudeb Dasgupta, Virendra Singh, 2017-12-21 This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test VDAT 2017 held in Roorkee India in June July 2017 The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions The papers were organized in topical sections named digital design analog mixed signal VLSI testing devices and technology VLSI architectures emerging technologies and memory system design low power design and test RF circuits architecture and CAD and design verification *VLSI Design and Test* Anirban Sengupta, Sudeb Dasgupta, Virendra Singh, Rohit Sharma, Santosh Kumar Vishvakarma, 2019-08-17 This book constitutes the refereed proceedings of the 23st International Symposium on VLSI Design and Test VDAT 2019 held in Indore India in July 2019 The 63 full papers were carefully reviewed and selected from 199 submissions The papers are organized in topical sections named analog and mixed signal design computing architecture and security hardware design and optimization low power VLSI and memory design device modelling and hardware implementation **Design systems for VLSI circuits** Giovanni DeMicheli, Giovanni De Micheli, P. Antognetti, Alberto Sangiovanni-Vincentelli, 1987-07-31 Proceedings of the NATO Advanced

Study Institute L Aquila Italy July 7 18 1986 **Digital VLSI Design with Verilog** John Williams, 2008-06-06 Verilog and its usage has come a long way since its original invention in the mid 80s by Phil Moorby At the time the average design size was around ten thousand gates and simulation to validate the design was its primary usage But between then and now designs have increased dramatically in size and automatic logic synthesis from RTL has become the standard design flow for most design Indeed the language has evolved and been re standardized too Over the years many books have been written about Verilog My own coauthored with Phil Moorby had the goal of defining the language and its usage providing amply along the way It has been updated with new editions as the language and its usage evolved However this new book takes a very different and unique view that of the designer John Michael Williams has a long history of working and teaching in the field of IC and ASIC design He brings an in-depth presentation of Verilog and how to use it with logic synthesis tools no other Verilog book has dealt with this topic as deeply as he has If you need to learn Verilog and get up to speed quickly to use it for synthesis this book is for you It is sectioned around a set of lessons including presentation and explanation of new concepts and approaches to design along with lab sessions *BSSC Inter Level Mains Exam | 2000+ Solved Questions [16 Mock Tests (8 Paper-I + 8 Paper-II)]* EduGorilla Prep Experts, 2022-08-03 Best Selling Book in English Edition for BSSC Inter Level Mains Exam with objective type questions as per the latest syllabus given by the Bihar SSC Compare your performance with other students using Smart Answer Sheets in EduGorilla's BSSC Inter Level Mains Exam Practice Kit BSSC Inter Level Mains Exam Preparation Kit comes with 16 Mock Tests 8 Tests of Paper I 8 Tests of Paper II with the best quality content Increase your chances of selection by 14X BSSC Inter Level Mains Exam Prep Kit comes with well structured and 100% detailed solutions for all the questions Clear exam with good grades using thoroughly Researched Content by experts **VLSI Design Methodologies for Digital Signal Processing Architectures** Magdy A. Bayoumi, 2012-12-06 Designing VLSI systems represents a challenging task It is a transformation among different specifications corresponding to different levels of design abstraction behavioral structural and physical The behavioral level describes the functionality of the design It consists of two components static and dynamic The static component describes operations whereas the dynamic component describes sequencing and timing The structural level contains information about components control and connectivity The physical level describes the constraints that should be imposed on the floor plan the placement of components and the geometry of the design Constraints of area speed and power are also applied at this level To implement such multilevel transformation a design methodology should be devised taking into consideration the constraints limitations and properties of each level The mapping process between any of these domains is non isomorphic A single behavioral component may be transformed into more than one structural component Design methodologies are the most recent evolution in the design automation era which started off with the introduction and subsequent usage of module generation especially for regular structures such as PLAs and memories A design methodology should offer an integrated design system rather than a set of separate unrelated

routines and tools A general outline of a desired integrated design system is as follows Decide on a certain unified framework for all design levels Derive a design method based on this framework Create a design environment to implement this design method Scientific and Technical Aerospace Reports ,1994 *Digest of Technical Papers* ,2001 *Study of Engineering and Career* J Vinay Kumar,2018-04-20 There are many ways to apply knowledge to achieve a successful career Different people have used different ideologies get to the top What are the characteristics that will help you achieve success This book caters not only to students stepping into the engineering fields or the corporate world for the first time but also to those who are stuck in the wrong profession The book highlights the importance of knowing your field of education the importance of personality finding the right opportunity in different fields of work choosing the right first employer and other important decisions related to your career This book is an essential read for anyone who wants to enter the field of engineering The volume includes a good number of illustrations with detailed notes **A Collection of Technical Papers** ,1984

Applications of Computational Intelligence Alvaro David Orjuela-Cañón,Juan Carlos Figueroa-García,Julián David Arias-Londoño,2018-12-13 This book constitutes the thoroughly refereed proceedings of the First IEEE Colombian Conference ColCACI 2018 held in Medellin Colombia in May 2018 The 17 full papers presented were carefully reviewed and selected from 60 submissions The papers are organized in topical sections on artificial neural networks computational intelligence computer science **Concurrency 88** Friedrich H. Vogt,1988-10-12 This volume contains the proceedings of CONCURRENCY 88 an international conference on formal methods for distributed systems held October 18 19 1988 in Hamburg CONCURRENCY 88 responded to great interest in the field of formal methods as a means of mastering the complexity of distributed systems In addition the impulse was determined by the fact that the various methodological approaches such as constructive or property oriented methods have not had an extensive comparative analysis nor have they been investigated with respect to their possible integration and their practical implications The following topics were addressed Specification Languages Models for Distributed Systems Verification and Validation Knowledge Based Protocol Modeling Fault Tolerance Distributed Databases The volume contains 12 invited papers and 14 contributions selected by the program committee They were presented by authors from Austria the Federal Republic of Germany France Israel Italy the Netherlands the United Kingdom and the United States **Database Machines** Haran Boral,Pascal Faudemay,1989 This volume contains 24 papers presented at the Sixth International Workshop on Database Machines The papers cover a wide spectrum of topics including system architectures storage structures associative memory architectures memory resident systems deduction and retrospectives on maturing projects The nature of the papers is highly technical and presumes knowledge of database management systems and familiarity with database machines The book is representative of the dual trend in the field towards 1 search for new functionality and 2 attention to detail completeness and performance of prototype implementations **Management** ,1986 **Graph Drawing** Ulrik Brandes,Sabine Cornelsen,2011-02-10 This

volume constitutes the refereed proceedings of the 18th International Symposium on Graph Drawing GD 2010 held in Konstanz Germany during September 2010 The 30 revised full papers presented together with 5 revised short and 8 poster papers were carefully reviewed and selected from 77 submissions The volume also contains a detailed report about the 17th Annual Graph Drawing Contest held as a satellite event of GD 2010 Devoted both to theoretical advances as well as to implemented solutions the papers are concerned with the geometric representation of graphs and networks and are motivated by those applications where it is crucial to visualize structural information as graphs *Proceedings* Institute of Electrical and Electronics Engineers,1984

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